DESIGN AND PHASE-NOISE MODELING OF TEMPERATURE-COMPENSATED HIGH FREQUENCY MEMS-CMOS REFERENCE OSCILLATORS

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DESIGN AND PHASE-NOISE MODELING OF TEMPERATURE-COMPENSATED HIGH FREQUENCY MEMS-CMOS REFERENCE OSCILLATORS

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To my wife,

Hoda

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SUMMARY

Frequency reference oscillator is a critical component of modern radio transceivers. Currently, most reference oscillators are based on low-frequency quartz crystals that are inherently bulky and incompatible with standard micro-fabrication processes. Moreover, their frequency limitation (<200MHz) requires large up-conversion ratio in multi-gigahertz frequency synthesizers, which in turn, degrades the phase-noise. Recent advances in MEMS technology have made realization of high-frequency on-chip low phase-noise MEMS oscillators possible.

Although significant research has been directed toward replacing quartz crystal oscillators with integrated micromechanical oscillators, their phase-noise performance is not well modeled. In addition, little attention has been paid to developing electronic frequency tuning techniques to compensate for temperature/process variation and improve the absolute frequency accuracy.

The objective of this dissertation was to realize high-frequency temperature-compensated high-frequency (>100MHz) micromechanical oscillators and study their phase-noise performance. To this end, low-power low-noise CMOS transimpedance amplifiers (TIA) that employ novel gain and bandwidth enhancement techniques are interfaced with high frequency (>100MHz) micromechanical resonators. The oscillation frequency is varied by a tuning network that uses frequency tuning enhancement techniques to increase the tuning range with minimal effect on the phase-noise performance. Taking advantage of extended frequency tuning range, and on-chip temperature-compensation circuitry is

embedded with the sustaining circuitry to electronically temperature-compensate the oscillator. Finally, detailed study of the phase-noise in micromechanical oscillators is performed and analytical phase-noise models are derived.

CHAPTER 1: Introduction

This research study covers the design and implementation of high frequency (>100MHz) low phase-noise temperature-compensated integrated micromechanical reference oscillators that are intended as primary replacement for low frequency quartz crystal reference oscillators in multi-gigahertz OFDM-based 3G and 4G wireless radio transceivers. The oscillators rely on both capacitively- and piezoelectrically-transduced bulk acoustic resonators as the resonating tank. Significant effort is made to explore low-power low-noise techniques that greatly increase both gain and 3-dB bandwidth (BW) of the CMOS sustaining amplifiers. Moreover, electronic frequency tuning techniques with minimal effect on the phase-noise performance are suggested and novel techniques to significantly improve the frequency tuning range in the presence of parasitic effects from the resonator are developed.

To improve the short-term temperature stability of the reference oscillator, an on-chip temperature compensation circuitry that extensively relies on the embedded frequency tuning capability of the oscillator is utilized. The output of the temperature compensation block that consists of an accurate temperature sensing unit and a control signal generation unit is appropriately scaled and applied to the frequency tuning network to electronically compensate for the temperature drift of the oscillator in commercial (-10ºC to 70ºC) and industrial (-40ºC to 85ºC) temperature ranges. Finally, the phase-noise performance of micromechanical oscillators is explored in detail. Among important factors the effect of different parasitic sources from resonator and sustaining amplifier including those caused

by the frequency tuning enhancement network on the phase-noise performance is studied and analytically modeled.

1.1 Origin and History of Reference Oscillators

Frequency reference oscillator is a pivotal block in the design of radio transceivers as it significantly affects the performance and size of the transceiver [1]. During the past three decades, the reference oscillators have been built based on high-Q quartz crystal oscillators [2]. Their superior stability and absolute frequency accuracy has allowed them to be the industry's preferred choice for frequency synthesis application (Fig. 1.1). However, emerging applications in electronic systems (and multi-mode radio frequency applications in particular) have created a number of challenges that can not be addressed by traditional quartz crystal reference oscillators.

Fig. 1.1. Miniaturized Quartz Crystal

Today's multi-gigahertz system-on-chip (SOC) applications require high frequency (>200MHz) integrated reference oscillators that exhibit similar phase-noise and stability performance to those of the quartz crystal oscillators. This is especially problematic for higher data transceivers that rely on OFDM-based 3G/4G standards whose error vector magnitude (EVM) requirements calls for very low phase-noise floor [3], [4]. The immediate implication for frequency synthesizers that use low-frequency quartz reference oscillators is to reduce the bandwidth of the loop filter to the point that accommodating

the filter on chip may not be practically feasible. Another shortcoming of quartz crystals is inherent incompatibility of their fabrication process with standard integrated circuits such as CMOS.

Micro-size quartz crystals have helped with reducing the overall form factor of quartz crystal reference oscillators in recent years. In addition, some companies have invested on integrating the quartz crystals in the same package with the rest of the electronic circuitry [5]. However, the oscillator is still large comparing to the other blocks of the single-chip transceiver fabricated in advanced CMOS processes. As the result, multi-mode radio transceivers have to rely on a single clock to deliver multiple reference frequencies with different phase-noise specification [3]. This difference in the phase-noise puts a strain on the frequency synthesizer. Micromechanical oscillators, on the other hand, offer significantly smaller form factor, higher frequency of operation, multi-mode operation, and potential integration with IC while delivering near-crystal phase-noise/jitter performance [6]-[8].

During the past two decades, researchers have focused on the application of micromechanical oscillators as replacement for low-frequency quartz crystal reference oscillators. The oscillators primarily rely on two types of micromechanical resonators: capacitively-transduced and piezoelectrically-transduced micromechanical resonators. Capacitive transducers create an electrical force that will be used to excite a particular resonance mode of the micromechanical structure. Piezoelectric micromechanical

resonators take advantage of electromechanical coupling caused by piezoelectric transduction in certain materials to excite the resonance mode of the structure.

A wide variety of capacitive micromechanical resonators have been used to build reference oscillators [9], [6], [8]. Earlier prototypes have extensively used flexural-mode capacitive beam resonators operating between 10kHz to 10MHz [9]. More recent work has extended the frequency range into the upper HF range (~20MHz) [10] (Fig. 1.2). The small power handling of beam resonators that is mainly due to its small mass combined with the reduced nonlinearity threshold caused by small gap size that forms the transducer negatively affects the phase-noise performance of the oscillator. In addition the need for automatic level control circuits used to keep the oscillation amplitude from reaching above the linear limit adds to the complexity of the system and further deteriorates the overall phase-noise performance of the oscillator [10].

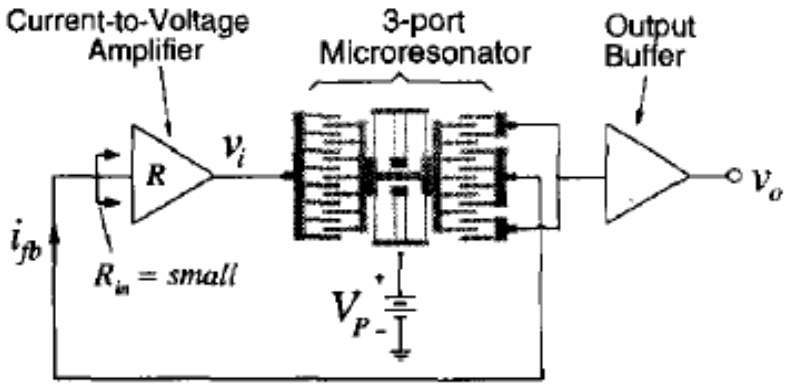


Fig. 1.2. Block diagram of 19MHz micromechanical oscillator [10]

Improvement to the design of the flexural beam resonators has resulted in significant increase in Q and power handling while preserving the large frequency tuning range of the resonator. The tuning range can be used to electronically compensate the frequency drift with temperature. In 2004, researchers at Discera, Inc. have reported a 70MHz

oscillator with simulated TCF below 0.2ppm/ºC with output power exceeding 0dBm and measured phase-noise ~-117dBc/Hz at 1kHz offset with floor reaching below -130dBc/Hz [11] (Fig. 1.3). The main disadvantage of using flexural beam resonators at high frequency is their high motional resistance (in this case ~16kΩ at V_p=7V) that requires electronics with large GBW that naturally include more active elements which exhibit more thermal and flicker noise. This increased noise content directly shows up in the phase-noise performance.

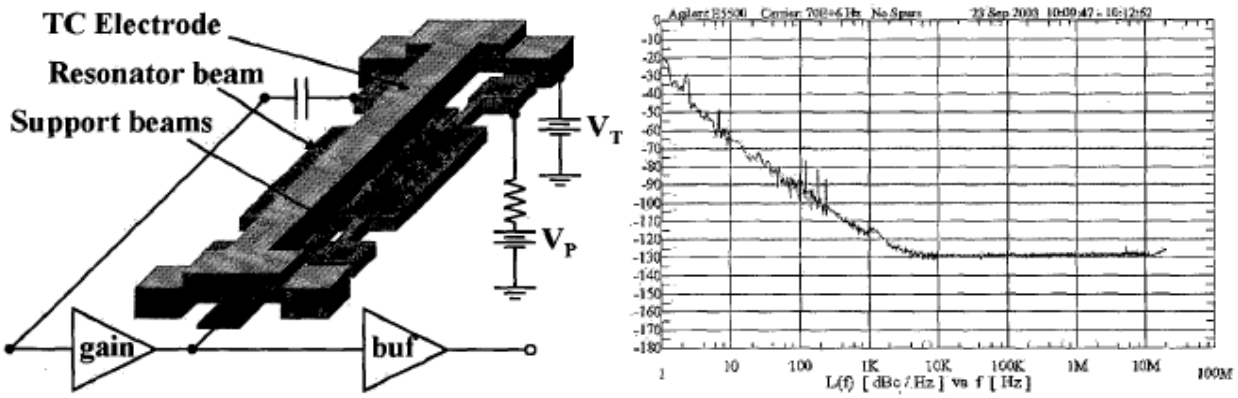


Fig. 1.3. Diagram and phase-noise of the temperature-stable 70MHz oscillator [11]

Another category of capacitive micromechanical oscillators use bulk acoustic wave resonators (BAW). These resonators excite an extensional bulk mode of the low-acoustic-loss material and exhibit larger mechanical stiffness and as such, have larger power handling capability [12]. In addition, they exhibit higher Q and lower loss, both critical for low-power low-phase noise oscillators. The fundamental resonance frequency for the majority of these BAW resonators is in the VHF range [8] but it has been shown that they can operate at much higher frequencies well into the UHF range [13], [14], [15] potentially extending the oscillation frequency beyond 1GHz [12], [6].

Bulk extensional mode devices originated with disk resonators in early 2000's [16] [17]. The early prototypes had high loss and therefore unsuitable for low-power oscillator applications. However, the eventual improvement in the performance (both Q and loss) led to the development of first capacitive micromechanical oscillator in VHF range at the University of Michigan [8] whose phase-noise performance was comparable with commercial quartz crystal oscillators. The resonator was a 60MHz wine glass disk resonator that was excited in its 2nd extensional mode and the sustaining amplifier was a simple fully-differential TIA fabricated in 0.35μm CMOS (Fig. 1.4).

More recent work has focused on using a micromachined silicon bar as a resonating material. These resonators are made of a relatively-thick single-crystal silicon bar that is separated from electrodes by very narrow capacitive gaps [18]. Called silicon bulk acoustic resonators (SiBAR), they offer similar Q but significantly smaller loss in upper VHF range [19].

Due to very large mechanical stiffness of BAW resonators, the electrostatic frequency tuning range is very limited [12]. As such, designers have been forced to search for alternative methods that enable sufficient tuning range for process/temperature compensation. A proven method is micro-oven control in which the resonator body is heated up by passing a controlled DC current through the resonator, thus changing its temperature-dependent resonance frequency [6]. While this method offers high accuracy (<±20ppm) and does not have a major impact on the phase-noise, its demand for high DC power (>50mW) makes it unattractive for many low power applications. A 103MHz

prototype temperature-compensated SiBAR oscillator is reported with phase-noise below -108dBc/Hz at 1kHz offset and total temperature drift of 39ppm in 100ºC (Fig. 1.5) [6].

To address the limitation in tuning range without sacrificing high Q and low loss of BAW resonators another category of BAW resonators that use a combination of bulk and flexural modes has been developed [20]. The device benefits from large flanges that are placed at the end of several extensional beams. These flanges increase the capacitive transduction area and hence increase the tuning range. Due to the specific geometry, these devices are called I-shaped Bulk Acoustic Resonator (IBAR). Tuning range approaching 5000ppm is reported for prototype in 5-20MHz [21] and is used for electrostatic temperature compensation (Fig. 1.6) [22]. The major problem with these resonators is their inherent limitation for frequency of operation that is a direct outcome of the mechanical design of the resonator.

State-of-the-art commercial capacitive micromechanical reference oscillators have been designed and optimized with the intention of competing with quartz crystal oscillators for variety of applications in consumer electronics, clock generation for computers, and communication [23]. As such, these reference oscillators are usually made with well-characterized low-frequency (<30MHz) capacitive resonators. Using single-chip programmable fractional-N frequency synthesizers, a wide range of frequencies have become available that greatly reduce the power consumption, size, cost, and complexity of the system [23]. Moreover, added functionality in the form of frequency tuning and process/temperature compensation can be available as well. More recent products take

advantage of four-terminal micromechanical resonators to deliver highly stable fully-differential programmable reference oscillators with lower jitter (Fig. 1.7) [23]. Still, due to the low frequency of the resonator, the phase-noise performance significantly deteriorates towards the higher-end of the frequency range (>300MHz) for large up-conversion ratios of the synthesizer. In addition, the need for vacuum packaging continues to be a major obstacle toward achieving very cheap micromechanical oscillators [24].

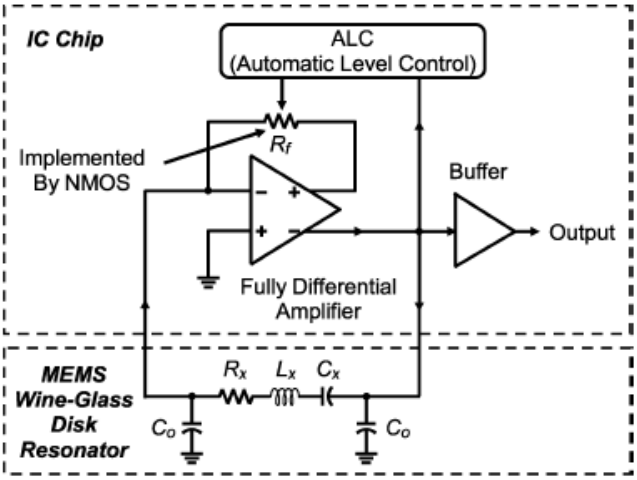


Fig. 1.4. Block diagram of 60MHz disk micromechanical oscillator [8]

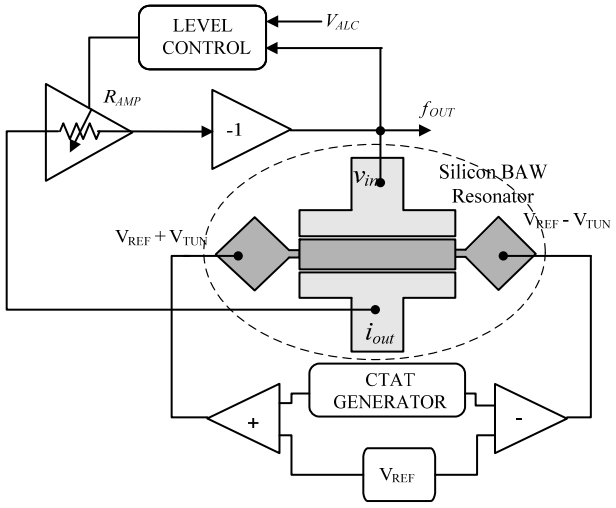


Fig. 1.5. Block diagram of 103MHz temperature-compensated SiBAR oscillator [6]

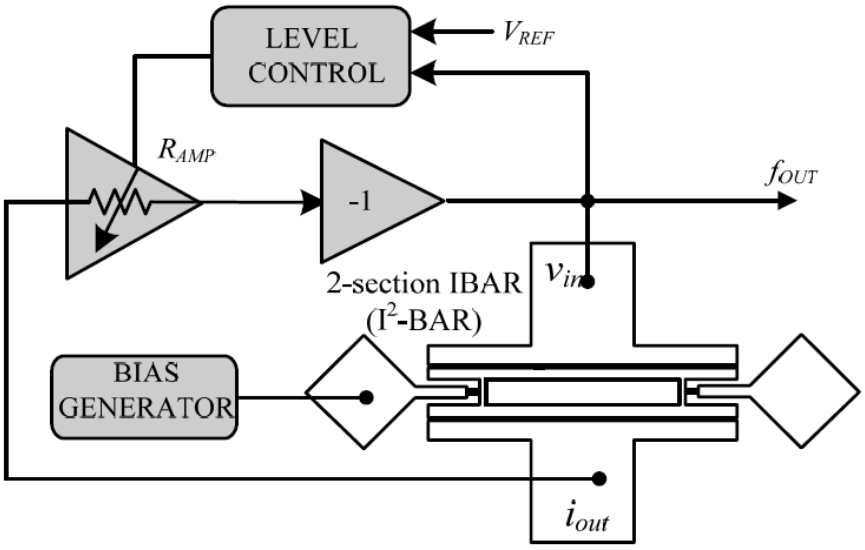


Fig. 1.6. General block diagram of temperature-compensated IBAR oscillator [22]

One of the biggest challenges in creating stable reference oscillators is to achieve frequency stability in presence of variations in process, temperature, and power supply. Most quartz crystal oscillators take advantage of high absolute frequency accuracy (<10ppm) and inherently-small temperature drift of the quartz crystal resonator (<100ppm in -40ºC to 85ºC) to deliver an accurate temperature- and process-insensitive clock [25]. However, for more accurate (<10ppm in -40ºC to 85ºC) crystal oscillators such as temperature-controlled crystal oscillators (TCXO), temperature and process compensation is necessary. The temperature compensation is usually achieved by accurately sensing the temperature variation and then adjusting the oscillation frequency [25]. For most applications, on-chip temperature sensors are sufficiently accurate. These sensors use bandgap and proportional-to-absolute temperature (PTAT) references to accurately predict the temperature difference.

Due to large temperature coefficient of frequency of most commercially-available micromechanical oscillators (|TCF|>25ppm/ºC), programmable micromechanical oscillators rely on closed-loop temperature compensation methods [26]. Closed-loop methods are usually built around the phase locked loop (PLL) that is readily available as part of the high-resolution fractional-N frequency synthesizers used in the programmable oscillators [23]. Therefore, the PLL-based closed-loop method is capable of providing ultra-stable oscillation with temperature drift less than 0.1ppm/ºC.

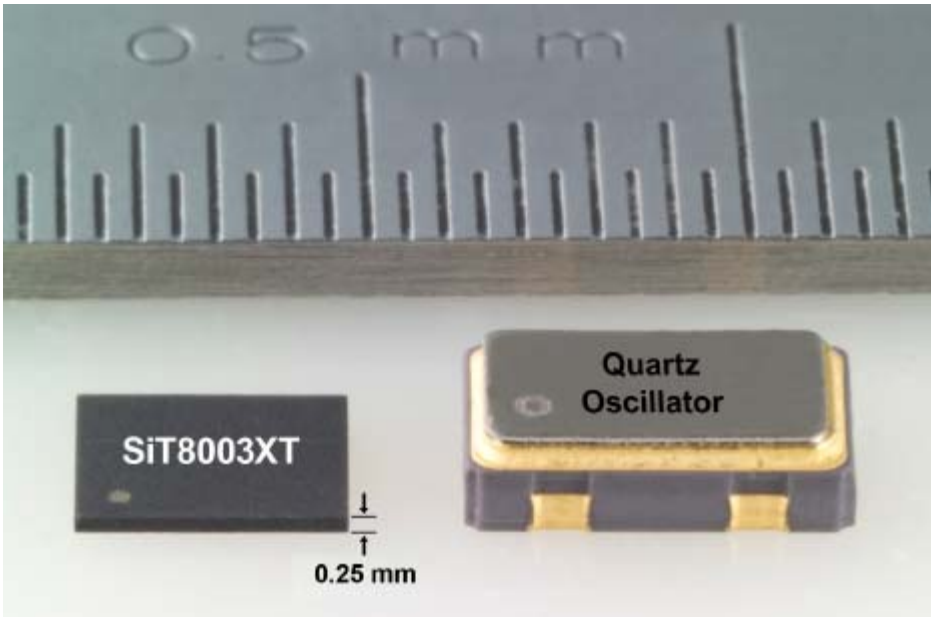


Fig. 1.7. SiTime's Ultra-thin high performance MEMS reference oscillator [23]

Piezoelectric micromechanical resonators can be traced back much further than capacitive resonators. The first prototypes were introduced in 1960's [27]. This is partly due to the fact that the principle of operation is similar to quartz crystals; they both take advantage of high electromechanical coupling in piezoelectric transduction. There are two important categories for piezoelectric resonators: bulk acoustic wave (BAW) [28] and surface acoustic wave (SAW) [29]. For a given area, the piezoelectric transduction is much larger than capacitive transduction. This larger force results in significantly lower

loss for piezoelectric resonators compared with their capacitive counterparts and makes them very attractive for low-power oscillator applications.

Piezoelectric micromechanical oscillators usually take advantage of resonators operating in a bulk mode for higher Q and hence, lower phase-noise [30]. Bulk mode resonators are divided into two categories: lateral and thickness-mode devices. Similar to capacitive resonators, an extensional mode is excited in lateral piezoelectric resonators [30]. Due to the limitation in the lithography, these resonators tend to operate at lower frequencies in the VHF range [31]. More recent work has pushed the resonance frequency of these resonators above gigahertz [32].

While high frequency piezoelectric SAW oscillators have been popular since the early 1980's [33], research on piezoelectric BAW oscillators made little progress until early 1990's [34]. Earlier versions primarily used think-film bulk acoustic resonators (FBAR) made of AlN that were designed for lower UHF range. The fabrication process of these resonators allows for integration with standard IC fabrication processes (Fig. 1.8) [34]. FBAR resonators enjoy very low loss (motional resistance < 10Ω) while maintaining high Q (>1000). This is a direct impact of high electromechanical coupling combined with large transduction area of the FBAR. The large area of FBAR gives rise to unwanted feedthrough coupling (usually in the form of capacitance) between the input and output terminals.

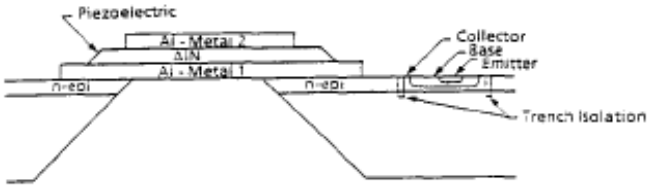


Fig. 1.8. Co-integration of thin-film bulk resonator with Si Bipolar process [34]

FBAR technology has made great strides to a state that commercial prototypes in upper UHF range are easily accessible in the market. The design of FBARs have been perfected for improved power handling that enables low phase-noise reference oscillators with high output power. Some researchers have shown that oscillators made with these resonators significantly outperform LC oscillators and can potentially meet the strict far-from-carrier phase-noise specification of broadband OFDM-based wireless standards such as 802.11n [35], [36]. A quadrature VCO oscillator based on a commercial 2.1GHz FBAR has been demonstrated and compared with an LC oscillator with on-chip passives in [36]. Incredibly-small loss of the FBAR has enabled sub-mW oscillator (~600μW) with phase-noise approaching -155dBc/Hz at 10MHz offset from carrier (Fig. 1.9). Considering the potential for post-CMOS fabrication compatibility of FBAR that uses AlN as piezoelectric transducer, FBAR oscillators can potentially compete with LC oscillators in delivering a fully on-chip solution for wireless standards. Still, one has to be mindful of relatively-poor close-to-carrier phase-noise performance in comparison with competitors such as crystal or capacitive micromechanical oscillator even when the synthesizer up-conversion is increased beyond 100.

Due to very low loss of FBAR, electronic frequency tuning is easier. The tuning, achieved by series tunable capacitors that introduce phase-shift in the loop, is usually

sufficient for temperature and process compensation [37]. This tunable capacitor can be integrated with the resonator [38] or can be placed on the sustaining amplifier [36]. In both cases, limited Q of these tunable capacitors significantly increases the Q loading in the oscillator and negatively affects the phase-noise performance. Material-based temperature compensation is also popular. Insertion of SiO_2 layer in the FBAR stack helps reduce the TCF but drastically reduces the Q for the thickness mode operation by as much as 3× [39].

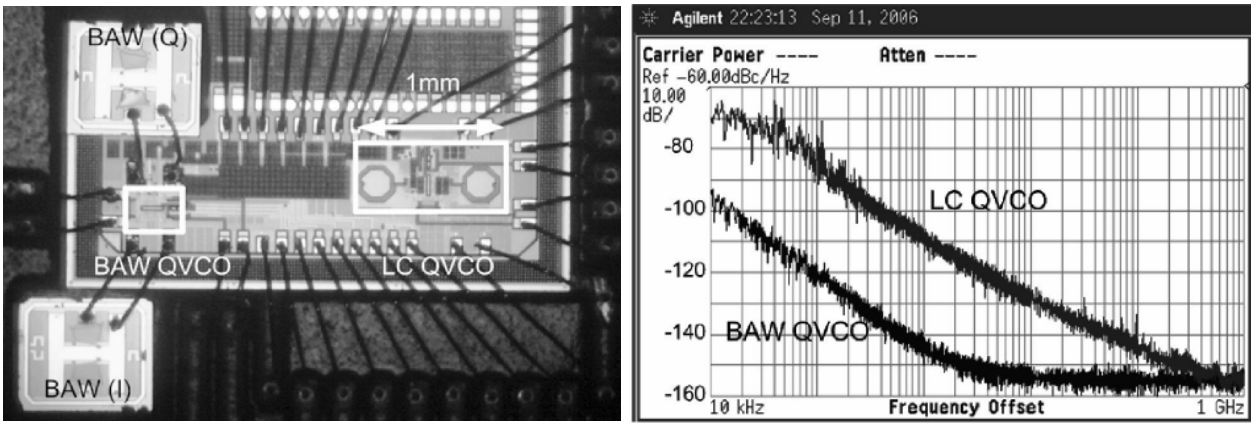


Fig. 1.9. 2.1GHz FBAR VCO and its phase-noise compared to an LC VCO [36]

The concept of lateral piezoelectric oscillators was first explored at very low frequency on cantilever beams. These resonators offered high Q (>1,000) and low loss but due to their very low resonance frequency (<100kHz), early prototypes were very large and naturally unsuitable for integration with IC [40]. Power handling was also a valid concern. Most of these low frequency resonators were fabricated on a thin substrate with low-stiffness. Therefore, the resonator threshold for nonlinear operation was low and the phase-noise performance of the oscillator was poor. In addition, some resonators were made of piezoelectric materials such as ZnO that are inherently incompatible with standard IC processes (Fig. 1.10) [40].

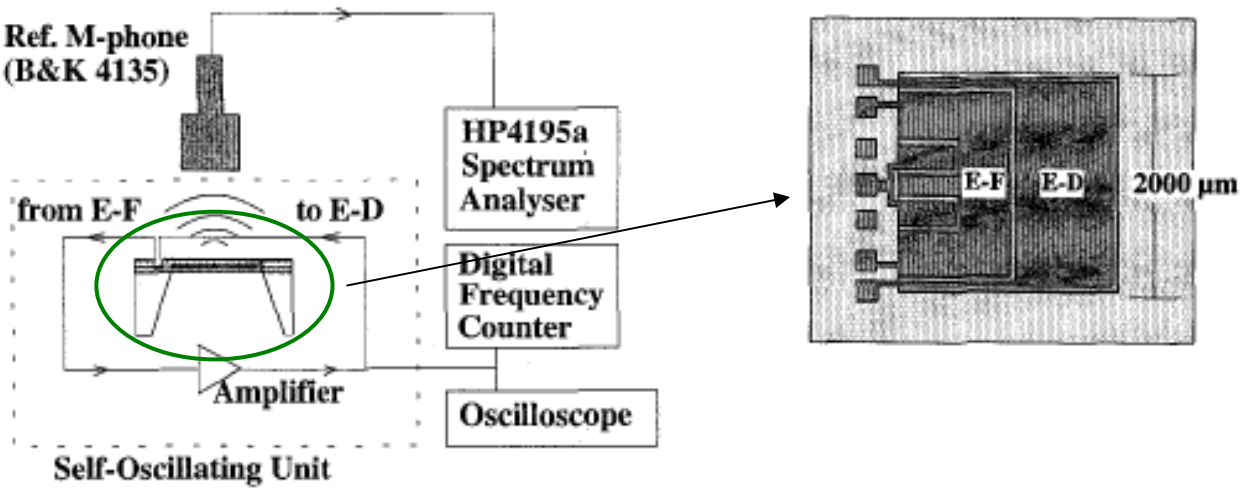


Fig. 1.10. Block diagram of the lateral piezoelectric oscillator [40]

The research continued on both low-frequency [41] and high-frequency laterally-excited piezoelectric resonators [42]. As discussed before, low frequency resonators were designed to replace quartz crystals. To this end, special effort was made to increase the Q and power handling capability, and reduce the loss [43]. Several categories of lateral piezoelectric resonators were explored [21], [44].

While operating in the first fundamental resonance mode of the structure seems to be a natural choice for many low frequency applications, it turns out that higher frequency modes of the same structure may provide similar f.Q at lower loss [21]. Most lateral piezoelectric resonators required reference electrode in addition to input and output electrodes. The reference electrode, commonly known as “reference ground”, was used to ensure all voltages on the resonator are properly referenced. This research resulted in piezoelectric oscillators in lower VHF range [44]. Several designs were studied to improve the Q and power handling and at the same time, reduce the loss of the resonator. Multi-finger topology was used to reduce the loss of the resonator by placing several

electrodes in parallel [30]. Another approach is to take advantage of mechanical coupling to increase the transduction area and reduce the loss without sacrificing the Q of the resonator. As an example an 81MHz oscillator based on a 12-resonator coupled array piezoelectric resonator is demonstrated. The resonator has unloaded Q of ~ 3,000 and motional resistance ~ 200Ω. The sustaining amplifier is a 2.2mW single-transistor NPN [44]. The oscillator achieves phase-noise better than -72dBc/Hz and -137dBc/Hz at 1kHz and 10MHz offset, respectively (Fig. 1.11). It is clearly shown that the power handling capability is improved compared to a multi-finger resonator [44]. An important advantage of thin-film piezoelectric-on-substrate (TPOS) resonators is that their fabrication process can be easily adapted to include a thin layer of SiO_2 layer that can be used for material-based passive temperature compensation [21]. Using a thin SiO_2 layer, the TCF of the 81MHz lateral piezoelectric oscillator is lowered to -2ppm/ºC (Fig. 1.12) [44].

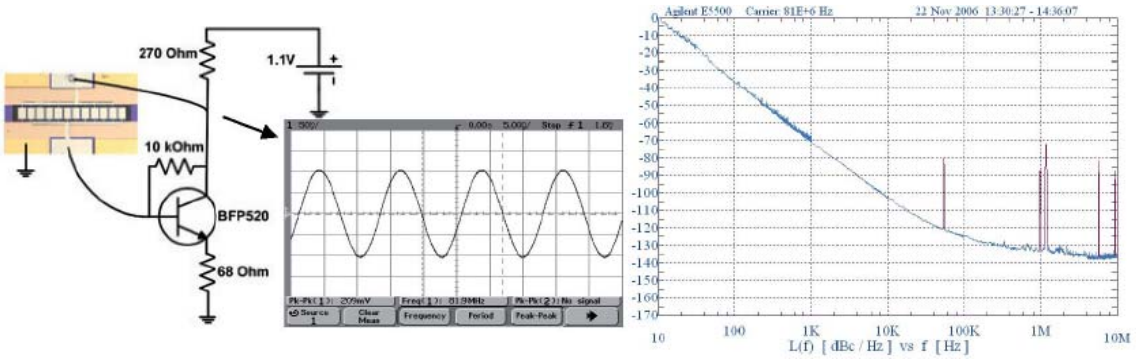


Fig. 1.11. Schematic and measured phase-noise of the 81MHz oscillator [44]

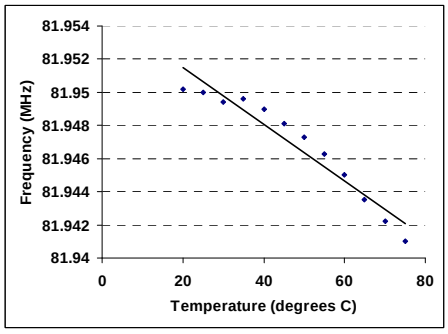


Fig. 1.12. Measured TCF of the 81MHz lateral piezoelectric oscillator [44]

Among lateral piezoelectric oscillators, contour mode AlN resonators have attracted a lot of attention [45] [46]. These resonators are capable of offering high power handling and high Q when integrated with CMOS electronics [45]. Researchers at Sandia National Laboratory have developed a single-chip multi-frequency AlN contour mode oscillator that operates at 20, 80 and 100MHz [45]. The phase-noise profile shows better than -90dBc/Hz at 1kHz offset for 100MHz oscillation (Fig. 1.13).

More recent studies have focused on pushing the frequency above 100MHz. The design of these resonators is very similar to low-frequency resonators except that the resonator is operated at higher width-extensional mode of the same structure [7], [46]. A 222MHz oscillator with phase-noise better than -88dBc/Hz at 1kHz offset and phase-noise floor approaching -160dBc/Hz is reported in [46]. The sustaining amplifier is a simple 10mW pierce topology that is fabricated in 0.5μm CMOS process. The lack of silicon substrate has reduced the power handling of the resonator below 0dBm. This reduced power handling, as expected, has a negative impact on the phase-noise performance of the oscillator (Fig. 1.14).

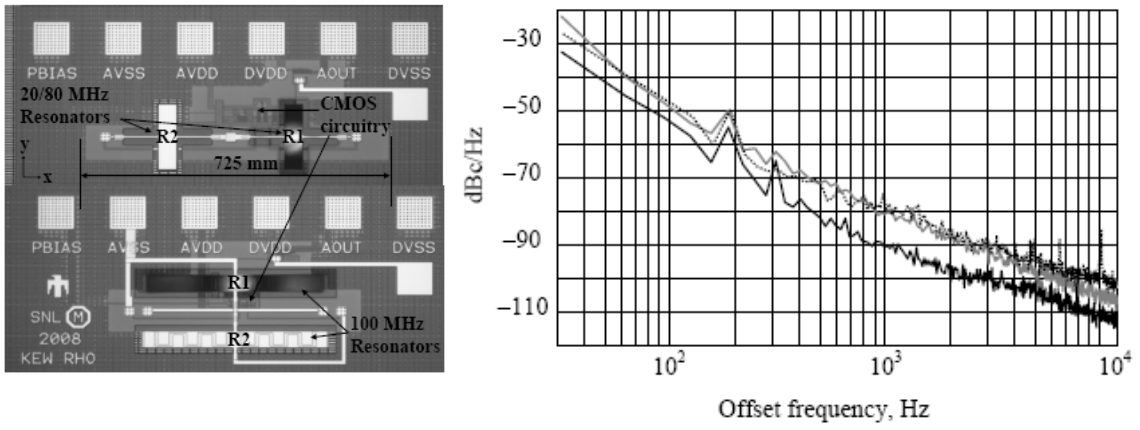


Fig. 1.13. Chip view and phase-noise of the multi-frequency ALN oscillator [45]

An important problem with lateral piezoelectric resonators is frequency tuning. Apart from limitation caused by the absence of polarization voltage in conventional piezoelectric transducers, lateral piezoelectric resonators usually suffer from large shunt parasitic capacitors to the reference electrode that seriously impede the realization of electronically-tuned piezoelectric micromechanical oscillators [47]. This is a much-needed first step toward fully temperature and process compensated lateral piezoelectric reference oscillator and a giant leap from current material-based temperature-compensated lateral piezoelectric reference oscillator [48].

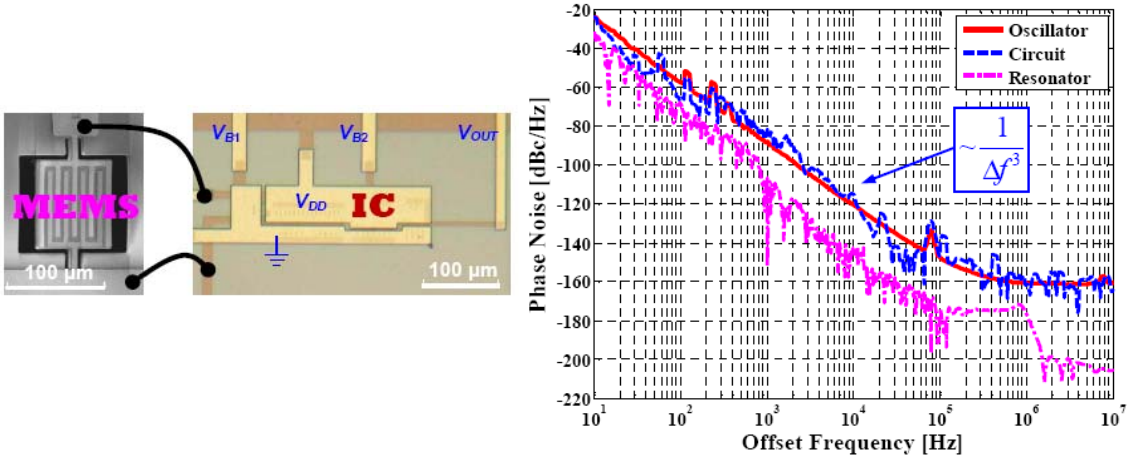


Fig. 1.14. View of the 222MHz oscillator and its measured phase-noise [46]

Although piezoelectric micromechanical oscillators present tremendous opportunity for delivering low jitter and low power frequency synthesizer solution for wireless applications, they have been largely ignored by industry. This could be due to the poor absolute frequency accuracy of the resonators at high frequency as well as their limited tuning range, esp. for lateral piezoelectric oscillator which makes it hard to compensate for temperature and process variation. The only exception is FBAR oscillators that are being considered as a possible alternative for low power single-chip medium performance oscillators for wireless applications. However, the excessive Q loading

caused due to very small motional resistance of FBAR device when interfaced with sustaining amplifier continues to be a challenge for achieving a phase-noise profile that is comparable to that of the up-converted quartz crystal oscillator.

1.2 Reference Oscillator Requirements and Classifications

There are several important characteristics for reference oscillators that are shared between micromechanical and other types of reference oscillators:

1.2.1 Short-Term Stability

Short-term stability is probably the single most important performance criterion of the oscillator and is a measure of frequency stability of the oscillator in steady-state operation. The short-term stability is usually expressed with phase-noise or jitter. The jitter is partitioned into two section random jitter (RJ) and deterministic jitter (DJ) and usually expressed in unit intervals (U.I.). Deterministic jitter is dependent to the data pattern dependant jitter and is attributed to a unique source. This type of jitter is usually not a source of concern in reference oscillators. The random jitter is due to the noise from electronics and typically exhibits a Gaussian distribution.

There are several different types of random jitter: absolute jitter, cycle-to-cycle jitter, periodic jitter, peak-to-peak jitter, edge-to-edge jitter, integrated jitter (frequency domain). The most important jitter quantities are absolute and cycle-to-cycle jitters. The absolute jitter is the instantaneous variation in oscillation frequency and for a periodic signal and its RMS value can be related to the phase-noise by [49]:

$$\Delta T_{abs,rms}^2 = \left(\frac{2\pi}{T_0}\right)^2 \int_{-\infty}^{+\infty} S_{\Phi n}(f).df \quad , \tag{1-1}$$

where $\Delta T_{abs,rms}$ is the RMS value of the absolute jitter, T_0 is the period of the oscillation, f is the frequency, and $S_{\Phi n}(f)$ is the power spectral density of the output signal at frequency "f". Examination of this formula reveals that the jitter is calculated from the equivalent area under the spectrum of Φ_n and then normalized to the period of oscillation. In other words, integrating the area under the phase-noise curve and then normalizing the result to T_0, gives out RMS value of the integrated jitter.

Cycle-to-cycle jitter of a free running oscillator can be related to its phase-noise by:

$$\Delta T_{cc}^2 \approx \left(\frac{4\pi}{\omega_0^3}\right) S_{\Phi}(f_m).df_m, \tag{1-2}$$

where ΔT_{cc} is the cycle-to-cycle jitter, ω_0 is the frequency of the oscillation, and $S_{\Phi}(f_m)$ is the relative phase-noise power at an offset frequency of "f_m". The important property of the cycle-to-cycle jitter that makes it a more accurate representation of oscillator short-term stability is the fact that it does not require a reference signal.

1.2.2 Long-Term Stability

Long-term stability is a measure of frequency stability over the factors influenced by the environment (such as temperature, humidity and acceleration) and time. The aging measurement is usually conducted by advanced tools that cycle the temperature according to a pre-specified test pattern. This pattern emulates the effect of aging for the oscillator. The response to humidity can be measured in a well-controlled humidity chamber. The frequency drift with temperature is usually expressed in ppm/ºC and is obtained with the help of a temperature chamber.

1.2.3 Absolute Frequency Accuracy

This is a measure of accuracy of the oscillation frequency and after short-term stability is the most important performance metric that is specified for reference oscillators. This quantity is usually expressed in ppm. There are several standards that each imposes a certain limitation on the maximum inaccuracy of the oscillator frequency. The majority of standards for consumer market put a cap on the total variation at 50ppm; however, there are some applications that can tolerate as much as 1000ppm. More demanding applications may require better than ±10ppm accuracy. As mentioned earlier, due to inherently low accuracy of most micromechanical oscillators, this level of accuracy usually calls for fractional-N frequency synthesizer solution.

1.2.4 Frequency Tuning

Frequency tuning is an essential property of every reference oscillator. This is necessary to adjust the oscillation frequency and potentially compensate for temperature and process variation. The tuning range is defined as the maximum range that the oscillation frequency can be systematically varied while still remains under control. Most micromechanical reference oscillators use a very stiff micromechanical resonator with limited tuning range below 1000ppm.

1.2.5 Waveform Shape

The oscillation waveform is typically a sinusoidal or a square. This shape is usually determined by nonlinearity of the oscillator that is influenced by a variety of factors including the circuit nonlinearity and resonator power handling. Most low phase-noise crystal or micromechanical reference oscillators deliver a near sinusoidal output waveform. Oscillation power is also important in determining the phase-noise performance of the oscillator.

1.2.6 Power Consumption

Power consumption of the oscillator is another key metric that has recently become an issue for integrated solutions in advanced IC processes where the reduction in supply voltage has pushed the overall power consumption down to a few milliwatt. Low frequency reference oscillators with power dissipation in the range of few tens of microwatt and gigahertz reference oscillators with power dissipation in the range of a few milliwatt are being explored for sensing and communication applications, respectively.

1.2.7 Size

The size requirement is mainly driven by the need for maximum integration. The integration with IC comes at a significant increase in cost which directly affects the commercial viability of the single-chip solution.

All of these criteria play a role, to a degree, in determining the performance of a reference oscillator. From a system designer's point of view, the designers should focus their efforts to maximize the short-term and long-term stability, tuning range and absolute frequency accuracy and at the same time minimize the size and power consumption. However, this task is proved to be more challenging than anticipated. There is a fundamental trade-off between stability and tuning range of the oscillator; a more stable oscillator tends to resist any change in the oscillation frequency. Moreover, the frequency accuracy is usually compromised for oscillators with very small form-factor due to the inherent inaccuracy of fabrication processes when dealing with small feature sizes.

Based on their performance, reference oscillators fall into one of these three categories:

- Low performance: low performance oscillators exhibit poor short-term and long-term stability as well as low frequency accuracy but they usually offer more flexibility in terms of frequency tuning, size, and power consumption. These reference oscillators are mainly intended as low-cost on-chip solutions with significant tuning range (usually more than 10%) and are available in a wide frequency range from a few kHz to tens of GHz. Famous examples are CMOS ring oscillator for low frequency and LC oscillator for high frequency that can be used to generate clock for microprocessors. A control signal is usually available to tune the frequency. For higher frequency, a control signal generation unit is used in a feedback loop to meet the required accuracy specification.

- High performance: high performance solutions are usually built around a crystal oscillator in PLL loop. High-Q micromechanical resonators (Q>50,000) have begun to replace quartz crystals as the preferred resonating tank in the reference oscillator for high-performance solutions. While these reference oscillators offer excellent stability (both short-term and long-term) and frequency accuracy, they are relatively large, especially in the case of quartz crystals that are off-chip, and very hard to tune. In addition, significantly higher power dissipated in PLL circuits makes them unattractive for low power applications. These solutions are ideal for wireless radio transceivers; for example, most cellular transceivers whether 2G or newer OFDM-based 3G systems rely on high performance quartz crystal oscillators to achieve ultra-low jitter performance [50]. The phase-noise requirements for some of the well-known cellular and broadband wireless standards are summarized in Table 1.1. From

Table 1.1, it is clear that reference oscillators used to generate clock for high data-rate cellular standards such as HSDPA with 16QAM or 64QAM modulation require some of the toughest close-to-carrier phase-noise specifications. However, the phase-noise requirements of older cellular standards such as GSM continue to pose a challenge for miniaturized and fully on-chip micromechanical reference oscillator solution.

Table 1.1. Phase-Noise Requirement for Cellular and Broadband Wireless Standards

Standard	Carrier Freq.	Modulation	Close-to-Carrier PN	Far-from-Carrier PN
GSM	900MHz	GMSK	-91dBc/Hz @1kHz [51]	-135dBc/Hz @3MHz [52]
WCDMA	2.1GHz	QPSK	-95dBc/Hz @1kHz	-134dBc/Hz @10MHz
HSDPA	1.7GHz to 2.1GHz	16QAM	-83dBc/Hz in-band [53]	-129dBc/Hz @10MHz [53]
802.11n	2.4GHz	64QAM	-91dBc/Hz in-band	-126dBc/Hz @20MHz
WiMax	2.3GHz	64QAM	-95dBc/Hz in-band	-132dBc/Hz @20MHz

Another application of high performance frequency reference oscillators is the clock for data converters [54]. The clock jitter limits the overall SNR of the data converter and sets an upper limit to the effective number of bits. In advanced communication transceiver systems, designers usually partition the total jitter budget into several parts and allocate a jitter budget for the ADC. Fig. 1.15 illustrates the challenges posed by clock jitter in increasing the resolution and speed of data converters. It is clear that high-speed ADC with conversion rate over 300MS/s can only tolerate a very small clock jitter of less than 0.5ps to achieve 10 bit accuracy. This stringent specification require a high performance clock with excellent short-term stability whose design is further complicated for micromechanical resonators with significantly higher loss than quartz crystals. From Fig. 1.15, a 300MS/s 10bit

Nyquist converter requires a high frequency micromechanical reference oscillator with Q in the range of 20,000.

For an ADC, the total SNR degradation of an ADC can be expressed as:

$$SNR(\deg radation) = 20\log_{10}\left(10^{-SNR_{ADC}/20} + 10^{-SNR_{Jitter}/20}\right), \tag{1-3}$$

where SNR_{Jitter} is the SNR of the ADC due to the clock jitter. The theoretical limit on SNR_{Jitter} is given by:

$$\Delta T_{rms} = \frac{10^{\frac{-SNR_{Jitter,dB}}{20}}}{2\pi f_{osc}}, \tag{1-4}$$

where f_{osc} is the clock frequency.

The relationship between the total phase jitter of the reference clock and the phase-noise can be expressed as:

$$\Delta T_{phase}^2 = \frac{2}{(2\pi f_{osc})^2}\int_0^{+\infty} L(f_m)\sin^2(2\pi f_m).df_m\ , \tag{1-5}$$

where $L(f_m)$ is the phase-noise at frequency "f_m" offset from carrier and for an oscillator that uses a resonator with a 2nd order bandpass response can be approximated by:

$$L(f_m) = \frac{FkT}{2P_{osc}}\left(1 + \frac{1}{f_m^2}.\left(\frac{f_{osc}}{2Q_{loaded}}\right)^2\right)\left(1 + \frac{f_\alpha}{f_m}\right)\ , \tag{1-6}$$

where F, k, T, P_{osc}, f_α, Q_{loaded}, and f_m are noise factor, Boltzman's constant, temperature (in Kelvin), power of the oscillation signal, a constant related to flicker noise corner, loaded Q of the resonator, and offset frequency.

- Medium performance: oscillators in this category stand in the middle between low performance and high performance oscillators. They offer extended tuning range and burn less power than the high performance oscillators but have worse jitter profile and frequency accuracy. Low frequency micromechanical reference oscillators that use lower Q (Q<10,000) but low loss (<100Ω) resonators fall in this category. These oscillators offer an ideal solution for wireline broadband data transfer applications. The jitter tolerance requirements for some of the well-known broadband optical standards based on GR-253-CORE SONET are listed in Table 1.2. These relatively relaxed requirements even allow for LC oscillators with on-board high-Q passives to be able to meet most of the jitter specifications shown in Table 1.2.

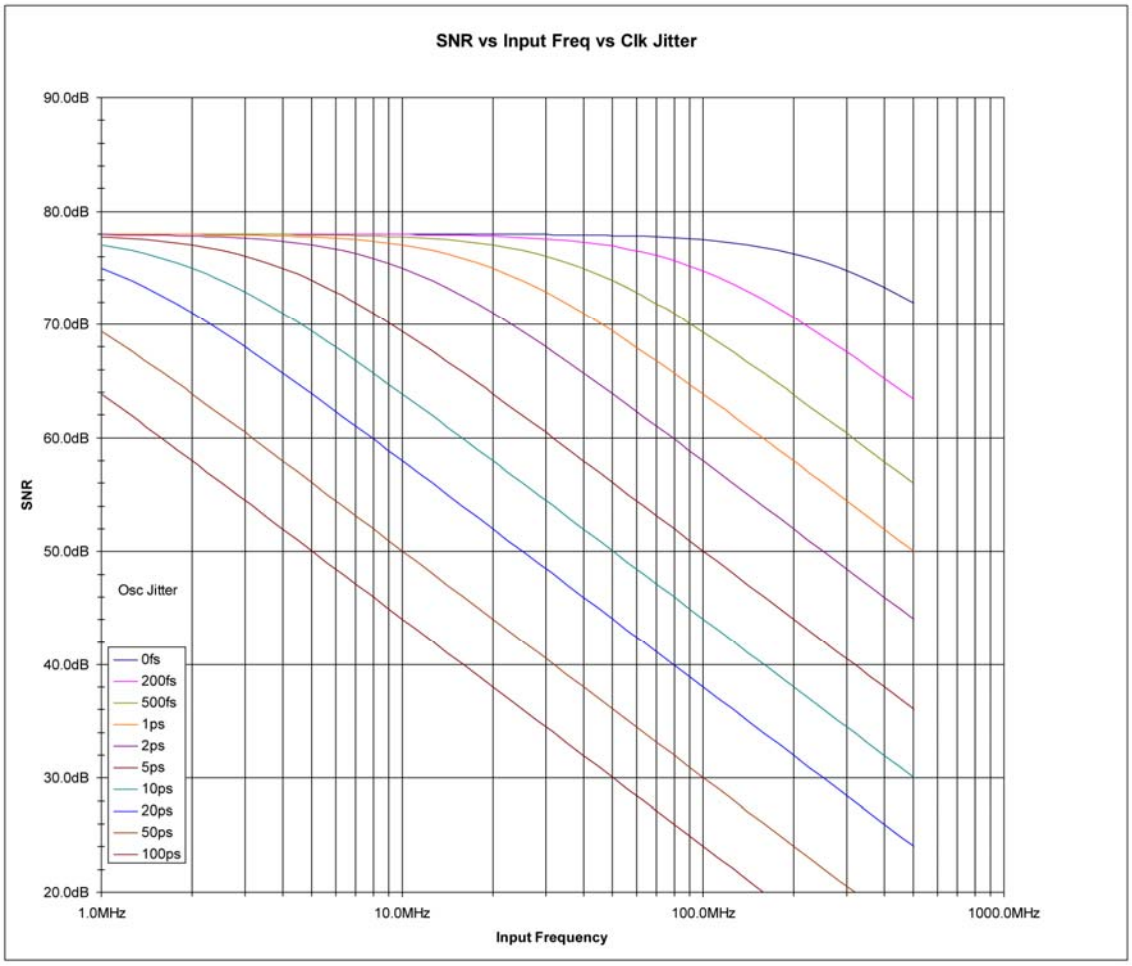


Fig. 1.15. SNR vs. clock jitter for ADCs [55]

Table 1.2. Jitter Requirement for Broadband Optical Standards

Standard	Rate	Close-To-Carrier Jitter (f_1)	Far-From-Carrier Jitter (f_2)
OC-12	622M	0.1 UI_{p-p} (10mUI_{RMS}) @12kHz	161UI_{p-p} (16.1UI_{RMS}) @5MHz
OC-48	2.5G	0.1 UI_{p-p} (10mUI_{RMS}) @12kHz	40.2UI_{p-p} (4.02UI_{RMS}) @20MHz
OC-192	10G	0.3 UI_{p-p} (30mUI_{RMS}) @20kHz	0.1UI_{p-p} (10mUI_{RMS}) @4MHz
OC-768	40G	6 UI_{p-p} (60m UI_{RMS}) @20kHz	0.15UI_{p-p} (15mUI_{RMS}) @16MHz

1.3 Organization

This dissertation is organized into seven chapters; Chapter 1 starts with brief introduction to micromechanical oscillators and their problem. It then briefly touches on the history of micromechanical oscillators and provides examples of the prior work. At the end, it proposes appropriate solutions for different applications and fits them into three performance categories. Chapter 2 discusses the fundamentals of micromechanical oscillators that include the sustaining amplifier, micromechanical resonator, and amplitude control unit. In this chapter the capacitive and piezoelectric micromechanical resonators and their electrical models are studied. Chapter 3 discusses the sustaining amplifier that is usually designed as transimpedance amplifier for series-resonant micromechanical oscillators. The topics covered in this chapter include open-loop and closed-loop TIAs and their frequency and noise response, low-power high performance techniques (both bandwidth and gain enhancement), design trade-offs, design examples and their measured performance and finally the comparison of different techniques. Tuning mechanisms for micromechanical oscillators are discussed in Chapter 4. The discussion starts with general description of the tuning methods for micromechanical oscillators that includes both resonator-based and electronic tuning. Examples of prior art are also provided as supplement to this section. The remainder of this chapter focuses on electronic tuning mechanisms for micromechanical oscillators, esp. those based on lateral micromechanical resonators. The discussion starts with the fundamentals of series and parallel tuning and inherent limitations on tuning range that is faced when applying these techniques to high frequency lateral micromechanical oscillators. The solutions to these shortcomings that significantly enhance the tuning range are then proposed. Finally, the

measured data which that validates the feasibility of these tuning enhancement techniques to increase the tuning range of high frequency micromechanical oscillators, is provided.

Chapter 5 covers the application of frequency tuning for micromechanical oscillators. It starts by providing a brief explanation of the fundamentals of on-chip temperature compensation for micromechanical oscillators and provides examples of prior work on temperature-compensated capacitive and piezoelectric micromechanical oscillators. After that, it goes into more details of each block such as temperature sensors, scalars, amplifiers, analog function generators and biasing circuits. The application of this technique to deliver electronically temperature-compensated high-frequency micromechanical oscillators is demonstrated by providing the measurement data for several oscillators. The last portion deals with the major sources of error and limitations in each block, and identifies approaches that help improve the absolute accuracy of the temperature compensation block.

The phase-noise of both capacitive and piezoelectric micromechanical oscillators are covered in Chapter 6. This chapter starts by providing an overview of the linear time-invariant (LTI) theory of phase-noise in oscillators with high-Q tank. Then, this theory is applied to a lateral micromechanical resonator. The effect of electronic thermal and 1/f noise on the phase-noise considered. Unlike prior published work, the effect of 2^{nd} order parasitics such as resonator and amplifier shunt parasitic impedances on the phase-noise performance, esp. close-to-carrier is studied in detail to arrive at a closed-form expression for overall phase-noise performance of the oscillator. In addition, the effect of resonator nonlinearity and other environmental parasitics such as temperature fluctuation and noise

from temperature compensation circuitry are discussed. Finally, measured phase-noise data from different micromechanical oscillators is used to support the theory. The phase-noise model is fitted to the data and any discrepancies are explained.

Chapter 7 lists the contributions of this work and provides a glimpse into the research work that is ahead for integrated high-frequency micromechanical oscillators to satisfy requirements for new demanding applications.

CHAPTER 2: High Frequency Micromechanical Oscillator Design

2.1 Introduction

As mentioned earlier, despite significant efforts toward integration of low-phase-noise reference oscillators on the same chip with modern radio transceivers, most systems continue to rely on large off-chip quartz crystal oscillators as the only viable solution for high-performance frequency synthesizers. However, the performance degradation caused by interconnects' parasitic (due to two-chip system) and large up-conversion ratio (due to the inherent frequency limitation of the quartz-crystal reference oscillator), as well as the desire to reduce the cost and size of the final product have motivated the designers to search for an integrated alternative to off-chip quartz crystal oscillators. Although miniaturized low phase-noise integrated micromechanical oscillators have been considered a potential candidate in crystal-less transceivers for several years, their low oscillation frequency has made them inferior to quartz crystals [22]. Recent progress in micromachining technology has accelerated the emergence of high-Q low-loss integrated micromechanical resonators as a feasible alternative to quartz crystals for communication transceiver applications [7].

Components used in a micromechanical oscillator will be studied in this chapter. These components include different types of resonators and electronic circuits that are used through this work. For each type of resonator, the principle of operation is briefly discussed and the procedure for lumped electrical modeling is explained. The required electronic circuits for micromechanical reference oscillators including the sustaining amplifier, temperature compensation circuitry and automatic level control, are identified

and briefly explained. Finally, examples of high frequency micromechanical oscillators are provided.

2.2 Micromechanical Reference Oscillator Block Diagram

A general block diagram of high frequency micromechanical reference oscillator is shown in Fig. 2.1. The block diagram consists of a sustaining amplifier, frequency tuning network, temperature sensing and compensation unit, on-chip buffer, and high frequency micromechanical resonator.

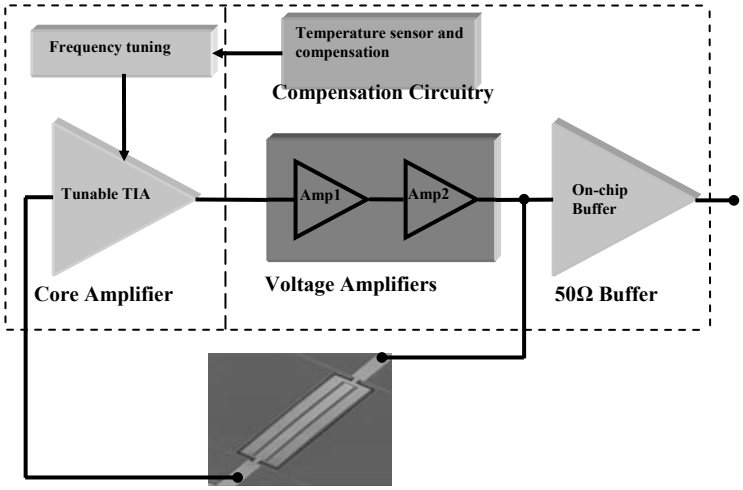


Fig. 2.1. General block diagram of high frequency micromechanical oscillator [1]

The sustaining amplifier is comprised of a tunable TIA and additional gain/phase-shift stages. The sustaining amplifier is mainly used to compensate for the loss of the micromechanical resonator and satisfy the Barkhausen's gain and phase criteria for oscillation [15]:

$$\left|A_{CL}(j\omega_0)\right| = 1, \tag{2.1}$$

$$\angle A_{CL}(j\omega_0) = 0, \tag{2.2}$$

where A_{CL} is the closed-loop gain and ω_0 is the oscillation frequency. The frequency of oscillation in determined by the resonance frequency of the micromechanical resonator:

$$\omega_0 = \frac{1}{\sqrt{L_m C_m}}, \tag{2.3}$$

where L_m and C_m are the equivalent inductance and capacitance in the resonator model.

The frequency tuning network is used to vary the frequency of oscillation. Temperature sensing and compensation unit provides a temperature dependent control signal that can be used to compensate for the frequency drift of the oscillator with temperature. High frequency micromechanical resonator acts as the frequency selective tank in the oscillator and sets the oscillation frequency. The on-chip buffer is used to drive the load that can be another block in the PLL or the input of measurement equipment.

2.3 Series-Resonant Micromechanical Resonator

Series-resonant micromechanical resonators are miniaturized mechanical resonant transducers that are actuated to resonate near their natural mechanical resonance frequency. This natural resonant frequency depends on the material and shape of the resonator. Micromechanical resonators usually consist of two parts: the transducer and mechanical resonant body. The transducer acts to convert the electrical energy to mechanical energy and vice versa; for most resonators the transducer interacts with "sense" and "drive" electrodes. The sense drive is usually at the input terminal of the resonator; it senses the electrical signal that is then converted to the mechanical domain. At the output terminal, the signal is converted back to electrical domain; then, the output load is driven by this electrical signal.

The frequency response of a micromechanical resonator operating close to its resonance frequency resembles that of a second-order linear time-invariant (LTI) system. The common electrical model used to describe a series-resonant micromechanical resonator consists of a series RLC network (Fig. 2.2) [56]. When both input and output terminals (electrodes) are in-phase and symmetric, the transformers can be eliminated.

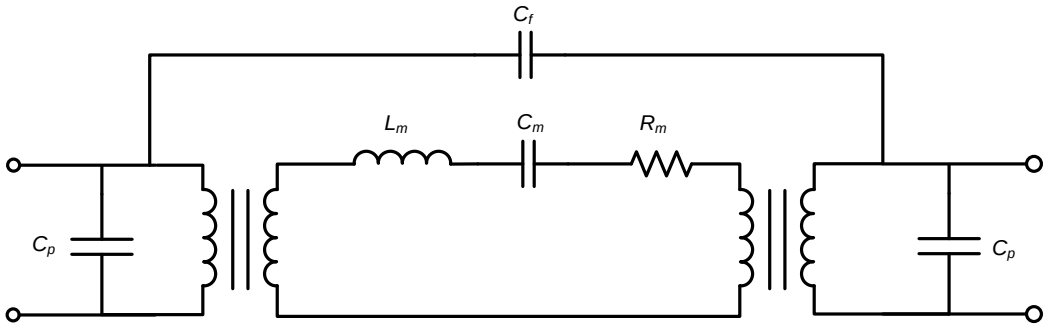


Fig. 2.2. Lumped RLC model for a series-resonant micromechanical resonator

For a single degree of freedom (SDOF) mechanical system such as micromechanical resonator, the resonance frequency is:

$$\omega = 2\pi f = \sqrt{K_{eff} M_{eff}^{-1}}, \tag{2.4}$$

where M_{eff} and K_{eff} are effective mass and effective stiffness, respectively. For a homogeneous and continuous system, M_{eff} and K_{eff} can be expressed as:

$$M_{eff} = \rho \frac{\int_V u^2(x, y, z) dV}{u_c^2}, \tag{2.5}$$

$$K_{eff} = \omega^2 M_{eff}, \tag{2.6}$$

where ρ is the density, $u(x,y,z)$ is the mode shape and u_c is the modal displacement at the point (x_c,y_c,z_c). Then, the parameters for the simplified series RLC electrical model of the micromechanical resonator can be derived as:

$$R_m = \frac{K_{eff}}{\omega Q \eta^2}, L_m = \frac{K_{eff}}{\eta^2}, C_m = \frac{\eta^2}{K_{eff}}, \quad (2.7)$$

where η is the electromechanical coupling coefficient, and R_m , L_m, and C_m are referred to as the motional resistance, motional inductance, and motional capacitance of the micromechanical resonator, respectively. At resonance, the effect of motional inductance and capacitance cancel out, leaving only the motional resistance that represents the minimum loss of the resonator across the frequency range.

Other parameters in the model are C_p that is the shunt parasitic capacitance at the input/output terminal of the resonator, and C_f that represents the feed-through path between the input and output node and is typically small for lateral micromechanical resonators (<50fF). The shunt parasitic capacitance includes both the capacitance from overlap between input/output electrodes and the reference electrode, and the capacitance from parasitic pads. The shunt parasitic capacitance could be as large as 4pF for some lateral micromechanical resonators.

2.3.1 Capacitive Micromechanical Resonator

The principle operation mechanism for this type of micromechanical resonators is capacitive transduction. Capacitive transduction creates an electrical force that will be used to excite a particular resonance mode of the micromechanical structure. To increase this force, a very narrow gap is formed between the electrodes and the body of the resonator. A polarization voltage is applied to the body of the resonator to avoid frequency doubling at the drive force and to create a sufficiently-large electric field for excitation. The material used in the fabrication of capacitive micromechanical resonators

are chosen such that the acoustic energy loss is minimized. For this reason, low-acoustic loss materials such as single-crystal silicon or nanocrystalline diamond are commonly used in combination with poly-silicon or poly-silicon germanium (poly-diamond). The capacitive micromechanical resonators usually exhibit very large Q (>50,000) [12] that is comparable to that of quartz crystals [57].

Although capacitive resonators exhibit very large Q, they suffer from large motional resistance. The motional resistance in these resonators is primarily limited by the polarization voltage that can be safely applied to them and the technology limit for the gap size. The motional resistance is inversely proportional to the capacitive gap size to the fourth power [56]. However, by optimizing the design and perfecting the fabrication procedure, low-loss high-frequency high-Q capacitive micromechanical resonators are within reach. Capacitive SiBARs are prime examples of optimized design and are the primary choice of micromechanical resonators that are used in high frequency capacitive micromechanical oscillators throughout this work. Fig. 2.3 shows an example of 103MHz high-Q (Q~92,000) capacitive SiBAR that is used in [6].

For a capacitive SiBAR operating in its fundamental width-extensional mode, the displacement of the resonator body toward the electrodes on its two sides is in phase [12]; as such, the direction of input and output currents is from the electrodes toward the resonator body. This shows that the input and output signals are 180º out-of-phase. This 180º phase difference from input to output can be modeled by an ideal inverting transformer (Fig. 2.4). The resonator-specific model parameters such as R_m, L_m, and C_m

can be obtained by fitting the RLC model to the measured frequency response for the resonator. Feedthrough capacitance, C_f, can be approximated by considering the level of isolation between input and output of the resonator.

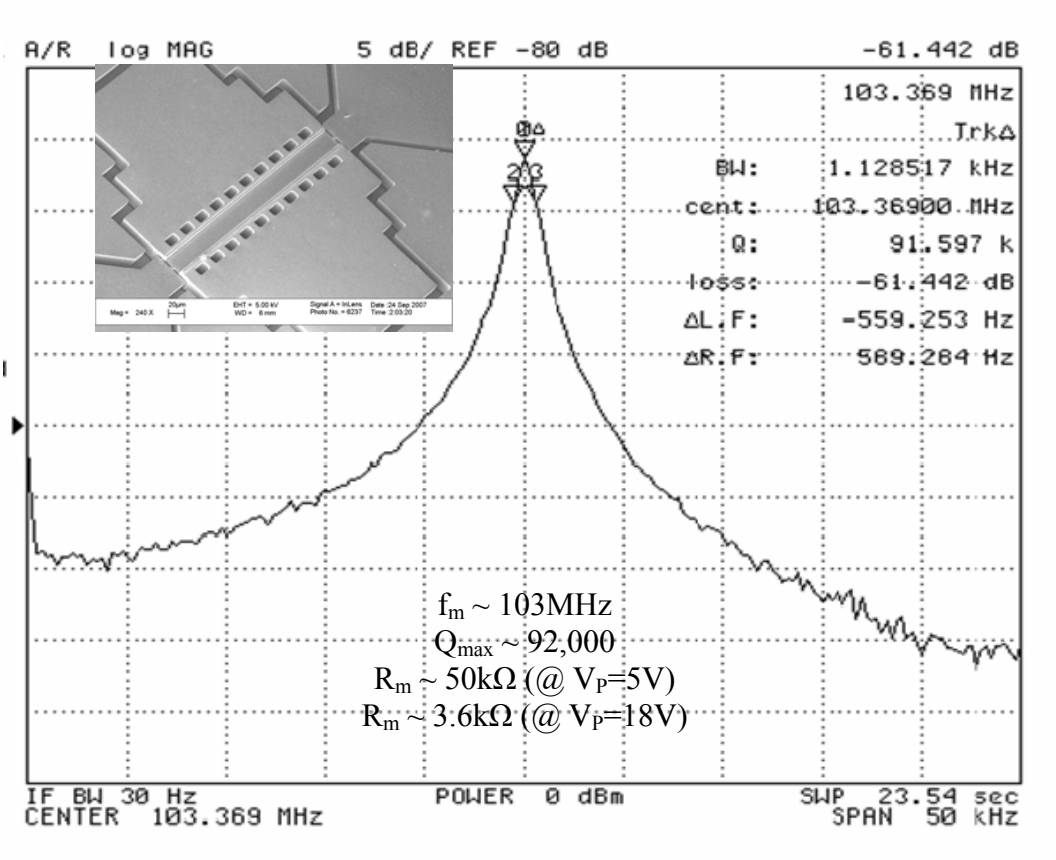


Fig. 2.3. The response and SEM of a capacitive micromechanical resonator [6]

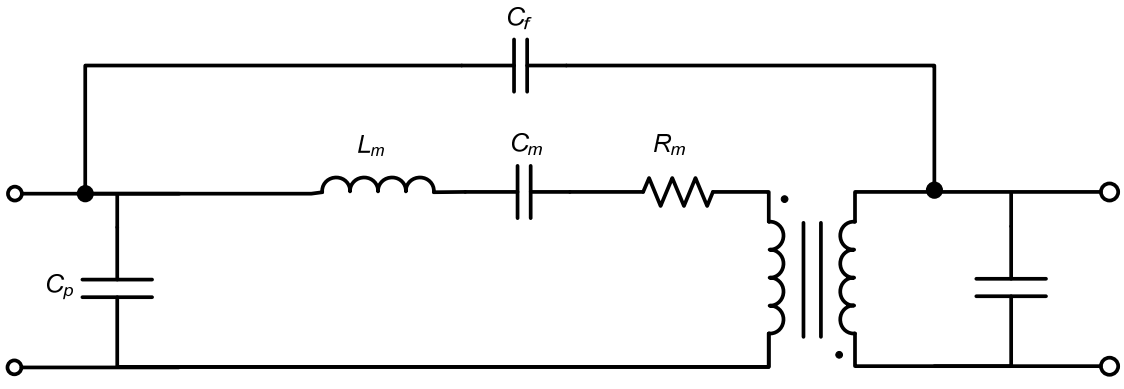


Fig. 2.4. Lumped RLC equivalent model for capacitive SiBAR

2.3.2 Piezoelectric Micromechanical Resonator

Piezoelectric micromechanical resonators take advantage of electromechanical coupling caused by piezoelectric transduction in certain materials to excite the resonance mode of the structure. As mentioned in previous chapter, most piezoelectric resonators are either categorized as bulk acoustic wave (BAW) [28] or surface acoustic wave (SAW) [29]. The electromechanical coupling of piezoelectric transduction is much larger than capacitive transduction; hence, when operating at the same frequency, the piezoelectricly-transduced micromechanical resonators exhibit significantly lower loss than their capacitive counterpart. This is particularly important for high frequency micromechanical oscillators where the loss of the resonator directly affects the power consumption and phase-noise performance.

Lateral piezoelectric resonators are typically constructed using a stack of multiple layers of materials that have different acoustic properties; in fact, some (such as metals) exhibit relatively high acoustic loss. Therefore, the reported Q from piezoelectric resonators is typically lower than those reported from capacitive resonators. The loss of acoustic energy at the interface of materials further reduces the Q of piezoelectric resonators. Despite this shortcoming, piezoelectric resonators usually outperform capacitive resonators in high frequency (>300MHz) oscillator applications due to their low motional resistance [7]. This study focuses on the application of high-frequency TPOS resonators to enable high frequency micromechanical oscillators in UHF range. Fig. 2.5 shows an example of 496MHz high-Q (Q~3,800) TPOS resonator that is used to deliver a low phase-noise micromechanical oscillator in [7].

Similar to capacitive SiBAR, the displacement of the body of a TPOS resonator operating in its fundamental width-extensional mode toward the electrodes on its two sides is in phase and hence, the direction of input and output currents is from the electrodes toward the resonator body. However, for operation in higher-order modes the displacement on two sides is opposite, so is the direction of input and output currents originating from electrodes. As such, the input and output signals are in-phase. This reduces the electrical model of a symmetric resonator to a simple RLC with parasitic (Fig. 2.6).

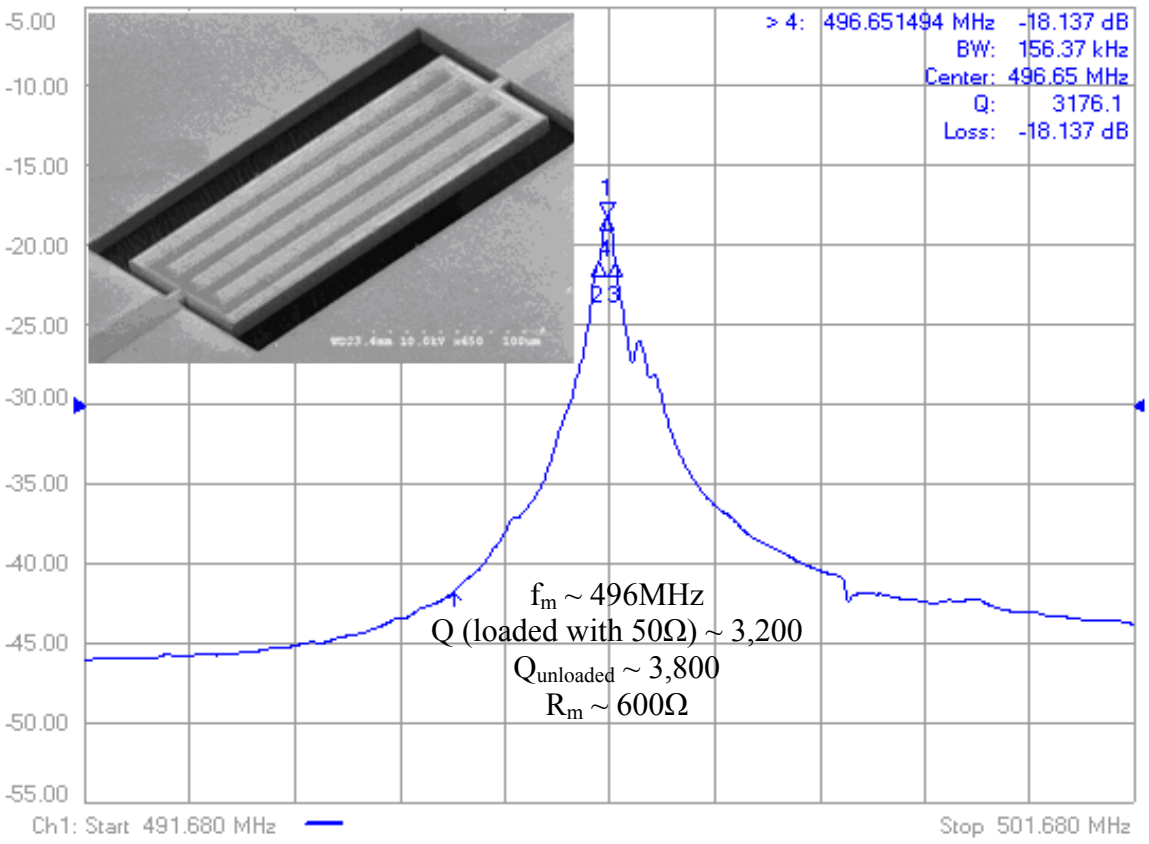


Fig. 2.5. Response and SEM of a 496MHz piezoelectric MEMS resonator [7]

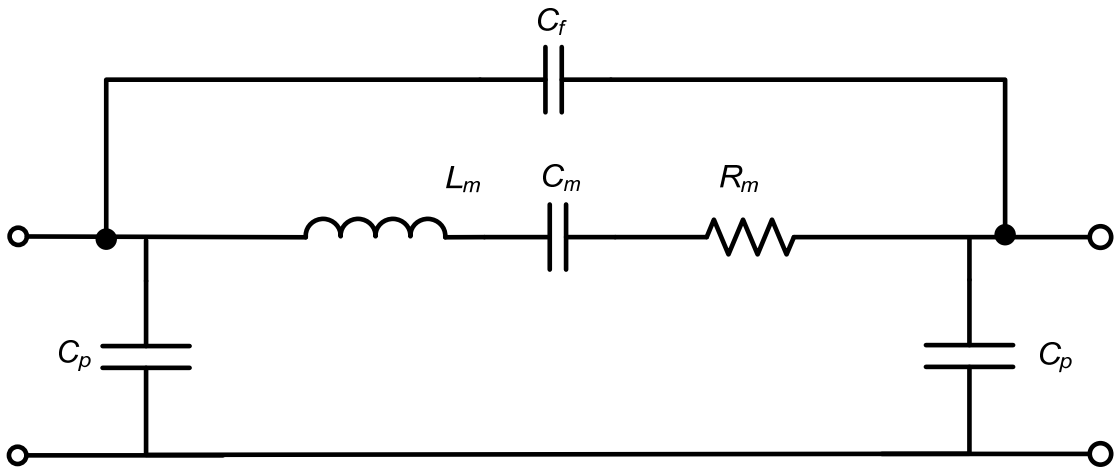


Fig. 2.6. Lumped RLC equivalent model for high-order TPOS resonator

2.4 Sustaining Amplifier for Micromechanical Oscillators

The sustaining amplifier is the main circuit block that provides the required gain and phase-shift to sustain the oscillation. There are usually two approaches to compensate for the loss of the micromechanical resonator in the oscillator loop: negative impedance generation and positive feedback loop.

In the negative impedance generation approach, the loss of the micromechanical resonator that is usually modeled by its motional resistance is cancelled through adding a negative resistance of equal size in parallel to the micromechanical resonator. This is because at resonance, the motional inductance, L_m, and motional capacitance, C_m, cancel out, leaving the motional resistance, R_m, which can be canceled by a negative resistance equal to "$-R_m$" that is generated by the negative resistance circuit (Fig. 2.7).

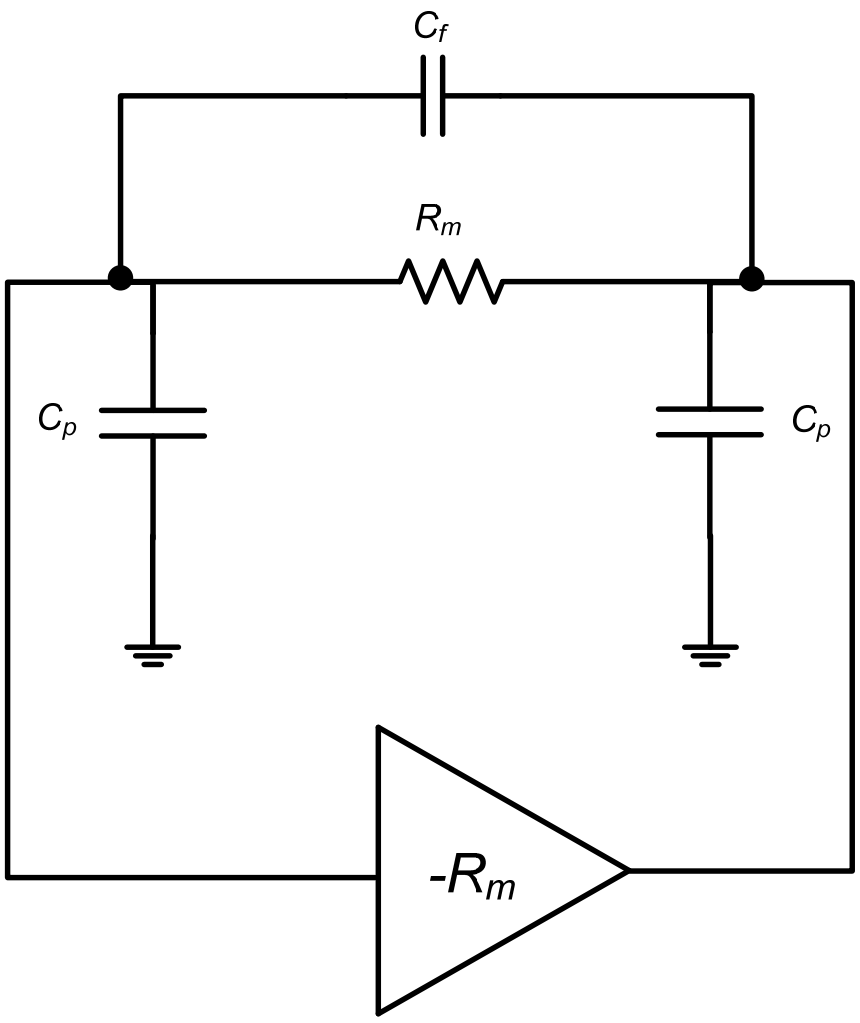


Fig. 2.7. Block diagram of the negative-resistance based micromechanical oscillator

There are quite a few topologies that can generate the required negative resistance and can be categorized into one-port and two-port negative resistance generators. One-port negative resistance generators are fairly simple and in some cases, can be built using a single transistor. Prime examples of this topology are Colpitts and Pierce oscillators. The latter is very popular in crystal oscillators and micromechanical oscillators that use low-loss resonators. Fig. 2.8 demonstrates the concept of negative resistance for crystal oscillator applications [58]. For most cases, the generated negative resistance can be related to the g_m of the transistor.

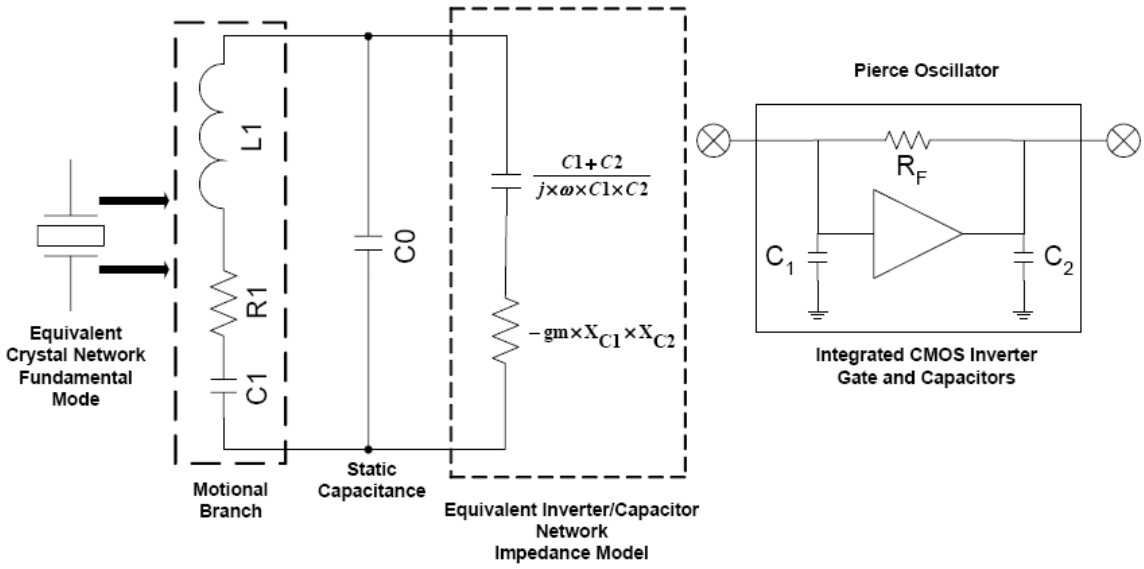


Fig. 2.8. Negative resistance model of a crystal oscillator [58]

Two-port negative resistance generators are slightly more complicated but they offer an advantage over one-port negative resistance generators; they can be made to operate differentially and therefore, are inherently more symmetric. However, this symmetry comes at a cost of more noise and higher power consumption. The cross-coupled topology is an example of pseudo-differential negative resistance generation topology that is widely used for high-frequency FBAR oscillators (Fig. 2.9). Addition of common-mode feedback to this topology can turn it into a fully-differential oscillator with outstanding phase-noise and harmonic rejection performance.

Although negative resistance-based oscillator topologies are inherently low power and hence, seem ideal for high frequency applications, the negative resistance that is generated in high frequency oscillators is relatively small. This is mainly due to the fact that the value of negative capacitance for majority of approaches is proportional to $1/g_m$ of the active devices. As the frequency of operation increases, so does the required

transition frequency (f_T) of the transistors which in turn, forces the designer to increase the g_m of the transistor in the face of constant parasitic capacitance. Larger g_m values translate to smaller negative resistance values which limits the application of negative resistance-based oscillation topologies for micromechanical resonators with high loss. For example, in frequencies above 1GHz, the value of negative resistance that is generated by cross-coupled topology is barely about -100Ω. This is about an order of magnitude smaller than the required negative resistance for gigahertz lateral micromechanical oscillators. On the other hand, the positive feedback approach can accommodate both low loss and high loss micromechanical resonators.

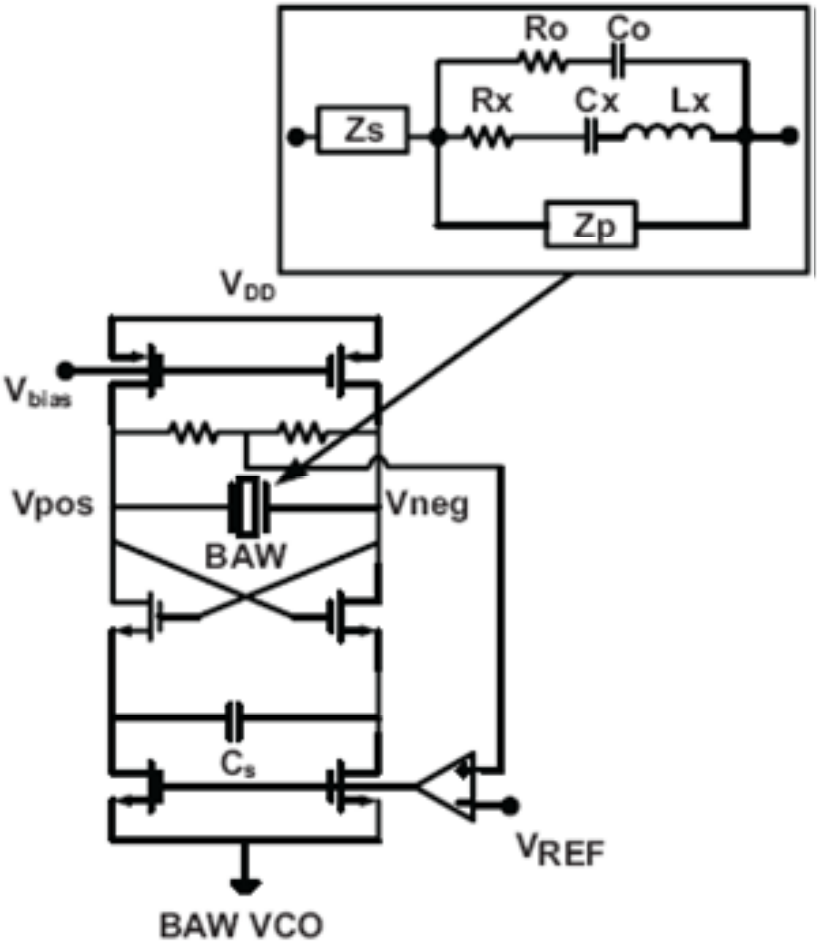


Fig. 2.9. Example of cross-coupled topology used in 2.1GHz FBAR oscillator [36]

In positive feedback approach, a sustaining amplifier is used with the resonator in a positive feedback loop to sustain the oscillation. For series-resonant micromechanical resonators, the output of the resonator is an AC current, therefore, the sustaining amplifier needs to simultaneously boost the input current and convert it to voltage at the output. This is done by a high-gain TIA.

An ideal TIA is a broadband amplifier with infinitely-small input and output impedances. TIAs are categorized into two general groups: open-loop and closed-loop (feedback) TIAs. Open-loop TIAs are based on a current amplifier in which the output current is passed through a resistance load to convert it to voltage. Closed-loop systems are usually built around a voltage amplifier with shunt-shunt feedback. The shunt-shunt feedback helps the output voltage track the input voltage by the ratio of the feedback resistance. In addition, it minimizes the Q-loading in the oscillator [8]. This resistance sets the transimpedance gain of the TIA and can be made tunable for greater flexibility.

In many cases, the power consumption and GBW requirements call for multi-stage TIA design. These TIA topologies usually take advantage of one or more voltage gain stages that provide additional gain and phase-shift that is required to satisfy Barkhausen's criteria for oscillation (Fig. 2.10). For high frequency applications, extreme care in the design of additional stages are necessary as these stage will appear as loading to the first stage and may limit the overall BW of the TIA.

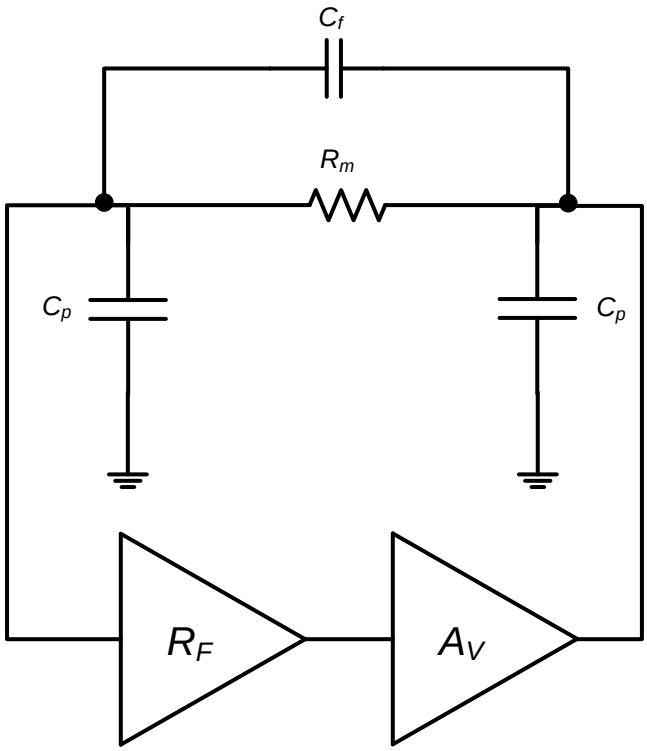


Fig. 2.10. Block diagram of the oscillator based on positive feedback loop with TIA

An example of a low-power 0.18μm CMOS TIA that is designed for high frequency capacitive micromechanical oscillator applications in shown in Fig. 2.11. The first stage is a common-source amplifier with tunable shunt-shunt feedback. This stage acts as the TIA. The second stage is also a common source with shunt-shunt resistive feedback. This stage acts as a low-power broadband voltage amplifier that provides additional gain. The shunt-shunt feedback in the second stage enhances the BW of the second stage in presence of large output load capacitance. The TIA consumes 2mA from 1.8V supply and achieves transimpedance gain > 80dBΩ with BW greater than 150MHz when loaded with 1.5F input and output capacitance [19] (Fig. 2.12). The gain can be tuned down more than 20dB. This TIA is interfaced with a 145MHz capacitive SiBAR that has a Q_{max}~74,000. The resulting phase-noise is better than -111dBc/Hz at 1kHz offset and meets the GSM phase-noise requirement.

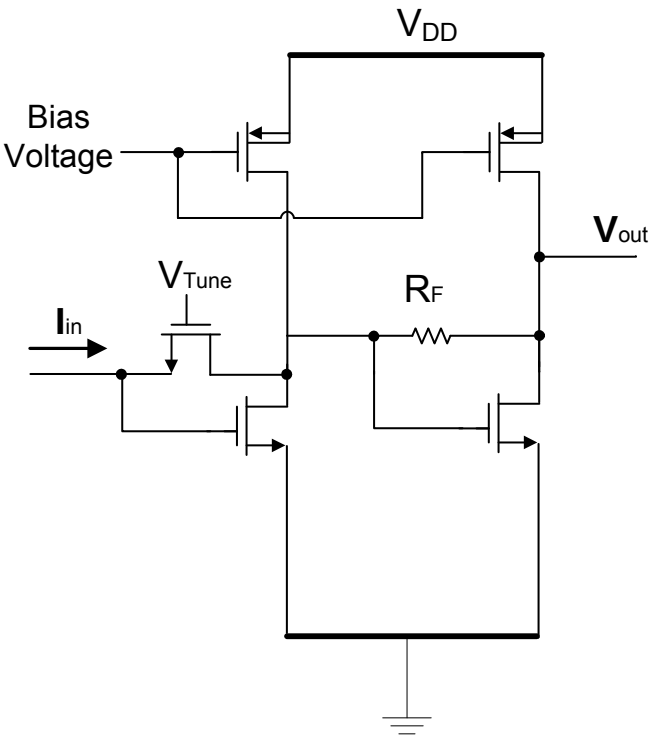


Fig. 2.11. Schematic of the two-stage 0.18µm CMOS TIA [19]

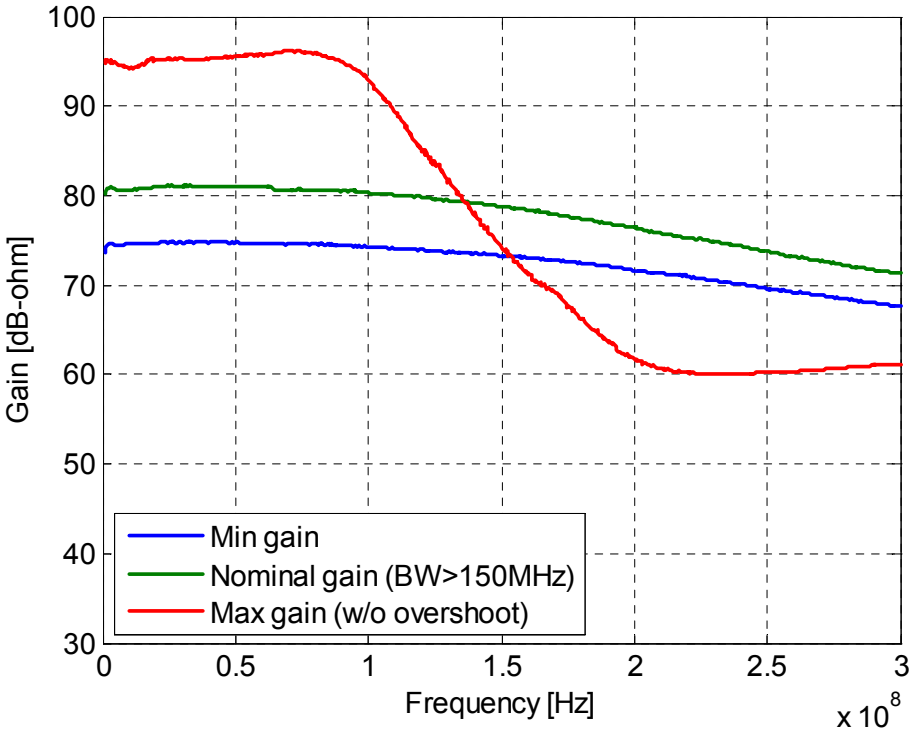


Fig. 2.12. Measured transimpedance gain of the two-stage 0.18µm CMOS TIA [19]

2.5 Automatic Level Control

Due to small power handling capability of some micromechanical resonators, an automatic level control (ALC) may be necessary to control the amplitude of the oscillation and prevent the micromechanical resonator to be derived into the nonlinear region. Nonlinearity of micromechanical resonators is the result of many factors including the resonator geometry, material, and transduction mechanism. The amplitude control is also essential in improving the close-to-carrier phase-noise performance of the oscillator. This is especially important for high frequency capacitive micromechanical oscillators where the requirement for small motional resistance calls for very narrow gaps that have a great impact on the linearity performance of the micromechanical resonator.

Fig. 2.13 shows a general block diagram of an ALC circuit that is used for micromechanical oscillators based on feedback TIAs [22]. Amplitude control is achieved by detecting the amplitude of the output signal with a high-speed peak detector and comparing the amplitude to a pre-defined resonator-specific threshold value V_{REF}. The value of V_{REF} is set by the nonlinearity limit of the micromechanical resonator. The resulting error signal is applied to the TIA to adjust the transimpedance gain with the help of a tunable MOS resistor. Varying the gain of the TIA affects the large-signal response of the oscillator which in turn, limits its output swing that is closely related to the amplitude of oscillation. For better accuracy, the ALC can be digitally programmed with the help of a high resolution digital to analog converter (DAC). Main limiting factors in this topology are offset of the comparator, speed of the comparator, and the accuracy of peak detector.

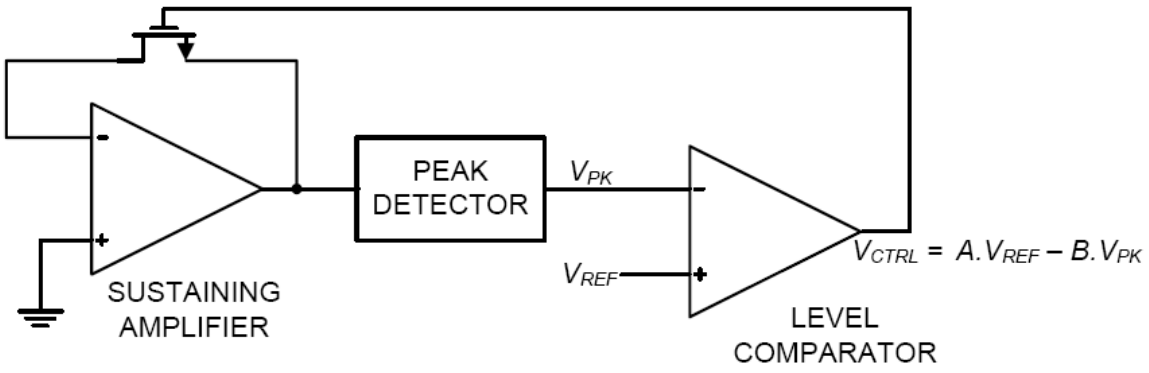


Fig. 2.13. General block diagram of ALC circuit [22]

Recent development in the design and technology of micromechanical resonators has increased their power handling capability that determines the threshold of nonlinearity. This is more pronounced in high frequency piezoelectric micromechanical resonators where the transduction area and resonating mass can be increased independently from the resonance frequency. This improved nonlinearity of the micromechanical resonator combined with constantly-shrinking supply voltage in advanced IC processes that severely limits the output swing has shifted the focus to sustaining amplifier as the main block that sets the amplitude of oscillation. Moreover, the ALC has negative effect on the phase-noise, especially close-to-carrier performance, of the micromechanical oscillator. As such, most high frequency (>300MHz) piezoelectric micromechanical oscillators do not use an ALC.

2.6 Temperature Compensation Circuit

Temperature compensation circuitry is an essential part of a micromechanical reference oscillator. Temperature compensation circuit consists of two blocks: temperature sensing and control unit, and analog function generator. The temperature sensing unit usually uses a temperature-insensitive block such as a bandgap reference, and a block whose

output varies linearly with temperature such as a proportional-to-absolute-temperature (PTAT) reference. The output of bandgap and PTAT references will be compared and scaled appropriately before being applied to an analog function generator. The analog function generator is designed to improve the performance of the temperature compensation block by trying to model the frequency vs. temperature behavior of the oscillator more accurately as this relationship is often times, nonlinear (Fig. 2.14).

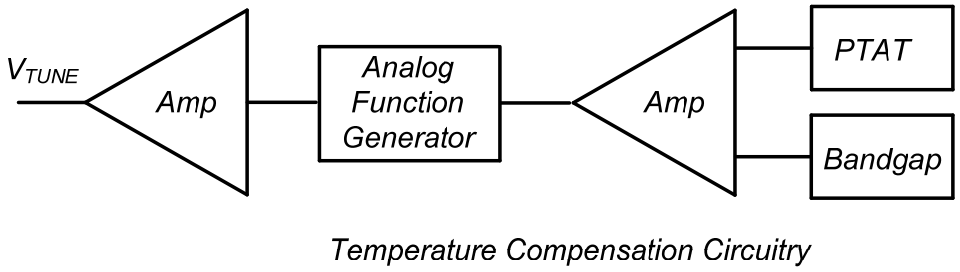


Fig. 2.14. General block diagram of the temperature compensation circuit

2.7 Micromechanical Oscillator Examples

Although both capacitive SiBAR and TPOS resonators are being used throughout this work, the major portion of this research study is dedicated to TPOS resonators as capacitive SiBARs have not yet been optimized (both in terms of loss and Q) to offer competitive solution for commercial frequency reference oscillators in UHF range. Still, efforts have been made throughout this study to increase the resonance frequency of the capacitive SiBAR with minimal effect on its Q and loss. In this section, examples of capacitive SiBAR and high frequency TPOS micromechanical oscillators are provided.

2.7.1 Capacitive SiBAR Oscillator

As mentioned earlier, High-Q capacitive micromechanical oscillators are viable timing solutions for modern communication systems as they offer superior close-to-carrier

phase-noise in a small form factor, and potential for integration with integrated circuits [6], [8]. This is achieved at the expense of higher power consumption and worse phase-noise floor, both of which are the result of high motional resistance of the capacitive transducer.

Temperature-compensated capacitive SiBAR oscillators have been successfully demonstrated in the past however, increasing the oscillation frequency has continued to be a challenge. The motional resistance of the capacitive micromechanical resonator increases rapidly as the frequency scales to the upper VHF [12], hence, making the resonator unsuitable for high frequency low power timing applications. The motional impedance can be minimized by increasing the transduction area or reducing the capacitive gap, both of which have practical limitations [12]. Simulation of the frequency response of a SiBAR in ANSYS reveals that there is an optimum thickness for which the motional impedance can be minimized.

The motional impedance is proportional to the fourth power of the gap, and inversely proportional to the square of V_p, and the transduction area A [18]:

$$R_m \propto \frac{g^4}{Q.V_p^2.A}, \tag{2.8}$$

Lowering the motional impedance of a device with given dimensions requires that either the gap size is reduced or V_p is increased. Both of these methods are unattractive due to the fabrication issues and inherent incompatibility of most IC technologies with high voltages. Therefore, increasing the transduction area (mainly through increasing the thickness of the resonator or by arraying resonators) or using a material with high

dielectric constant in the gap [15] appears to be the path toward lower motional impedance resonators. The latter, however, may negatively affect the Q and significantly increases the static capacitance of the resonator; thereby, making it unsuitable for low-power low phase-noise oscillators.

The value of the silicon thickness that minimizes the insertion loss (while keeping the thickness less than 30μm for ease of manufacturing) was determined from ANSYS simulations of a model of the complete device, including electromechanical transduction in the capacitive gaps. Different types of element models available in ANSYS were used for the various components of the resonator. A number of resistors and capacitors were also added to model the test setup used for resonator testing (Fig. 2.15). This model makes it possible to simulate the frequency response of a SiBARs of arbitrary dimensions.

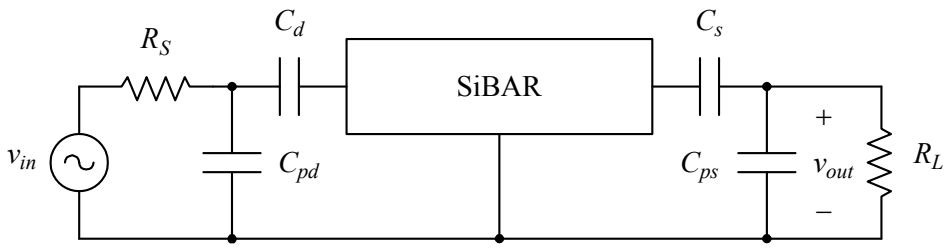


Fig. 2.15. Circuit equivalent of the ANSYS model of the SiBAR

Each simulation consists of a static analysis, which is needed to account for the effect of the DC polarization voltage, followed by a harmonic analysis over a specified frequency range. This particular set of analyses, combined with the inclusion of the electrostatic gap in model, provides more comprehensive and more accurate information about the behavior of the complete device than is obtainable from a simple modal analysis. In particular, the simulation results include the values of all node voltages, which makes it

possible to generate plots of the voltage gain $A_v = v_{out}/v_{in}$ over the specified range of frequencies. Several parameters indicative of the resonator performance can then be obtained from those plots, including the magnitude of the resonant peak, which is related to the insertion loss of the device.

Simulations of a set of SiBARs of fixed length (270μm) and width (27μm) were used to generate the plot in Fig. 2.16, which shows the values of $|A_v|$ at resonance as a function of device thickness. The optimal range of thickness values that minimizes the insertion loss in the device is clearly identifiable in the plot (15-20μm).

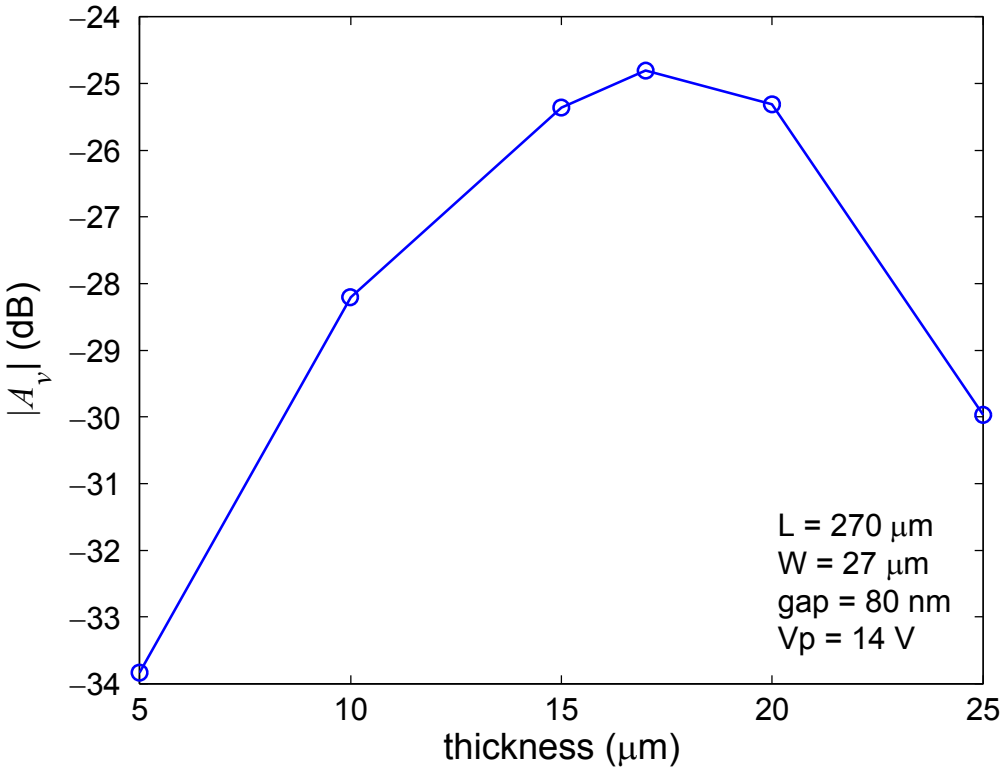


Fig. 2.16. Value of $|A_v|$ at resonance vs. device thickness

To validate the optimum thickness obtained from ANSYS simulation, a high-Q 270μm×27μm SiBAR was fabricated using the HARPSS process flow [12] on a p-type

SOI ultra-low resistivity silicon (0.005 Ω.cm) with 15μm thick device layer, as predicted by ANSYS simulation. The measured frequency response of the fabricated SiBAR shows maximum Q ~ 74,000 at 145MHz with V_p=2V (Fig. 2.17). The resulting $f.Q$ product, ~1.1×10^{13}, is comparable to that of quartz resonators (~1.6×10^{13}). After increasing V_p to 14V the motional impedance is reduced to 2.4kΩ (Fig. 2.18), which makes the device suitable for low-power oscillators. The drop in Q at higher V_p is attributed to a parasitic resistance, R_{load}, that appears in series with R_m in the equivalent electrical model:

$$\frac{Q_{res}}{Q_{measured}} \propto \frac{R_m + R_{load} + R_s}{R_m}, \tag{2.9}$$

where Q_{res} is the intrinsic mechanical Q of the resonator, R_s is the resistance of silicon bar, R_{load} is the parasitic series resistance that loads the Q, and R_m is the motional resistance of the resonator that becomes smaller with larger V_p. For this resonator, R_{load} is extracted to be ~1.07kΩ.

The sustaining amplifier is a two-stage feedback TIA (Fig. 2.11). Due to the large motional impedance and input/output parasitic capacitance of the resonator, unlike the TIAs used for low loss high frequency piezoelectric resonators, the TIA gain and 3dB bandwidth have to increase simultaneously. To increase the gain of the TIA beyond the required 80dBΩ without significant increase in power consumption, the signal is passed through additional voltage amplifier with fixed gain. Local shunt-shunt feedback is also used in this stage to improve the 3dB-bandwidth and linearity of the amplifier. The result is a two-stage amplifier in which the first stage uses common-source topology with tunable shunt-shunt feedback and acts as the TIA. The second stage provides additional voltage gain. The gain tuning is realized through an externally-controlled NMOS resistor.

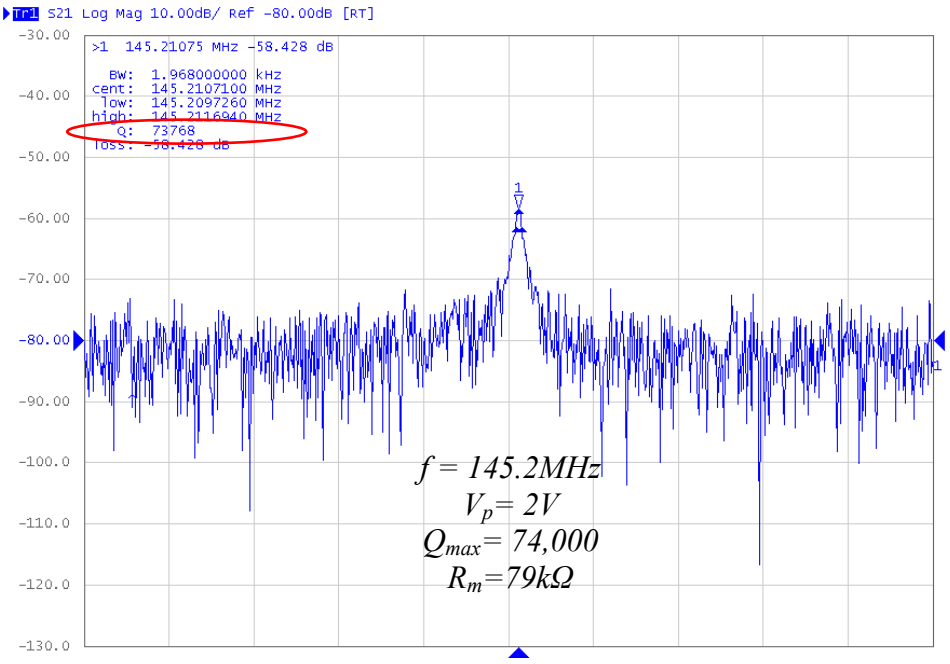


Fig. 2.17. Measured frequency response of the 145MHz SiBAR (highest Q).

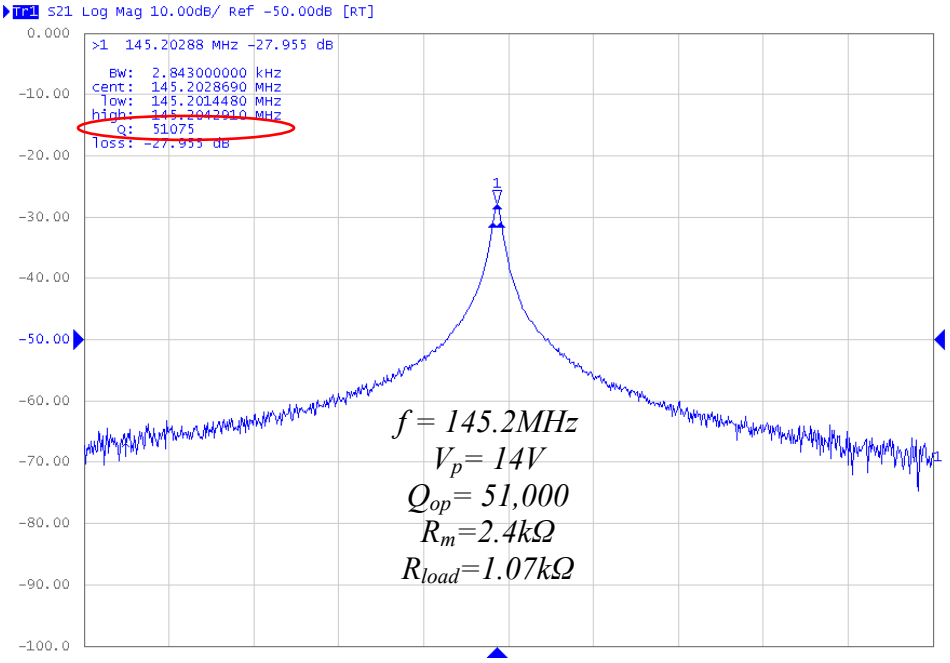


Fig. 2.18. Measured frequency response of the 145MHz SiBAR at V_p=14V.

The sustaining circuitry is fabricated in a 0.18µm 1P6M CMOS process and measures 600µm×300µm, of which only 70µm×40µm is occupied by the sustaining amplifier (Fig. 2.19). An off-chip 50Ω buffer is used to interface with measurement equipments. The

TIA provides more than 80dBΩ at 150MHz with 1.5pF input and output capacitance (equivalent parasitic capacitance of a SiBAR) while consuming 2mA from 1.8V supply. The gain can be tuned by more than 20dB from 75dBΩ to 95dBΩ (Fig. 2.12) before the appearance of peaking in the frequency response. At highest gain configuration (95 dBΩ), the BW is just under 100MHz with the same loading. The resonator and IC are interfaced through wirebond.

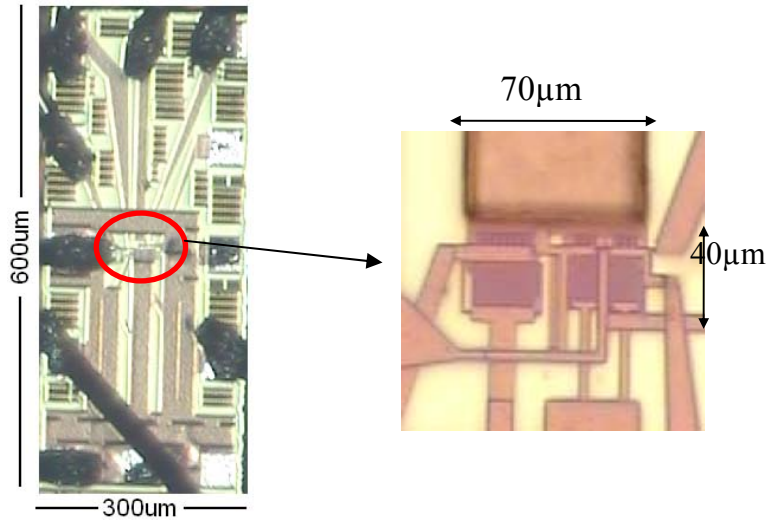


Fig. 2.19. Micrograph of CMOS TIA. Magnified view shows the active area.

The oscillator phase-noise is measured in vacuum using an Agilent E5500 phase-noise analyzer system. The measured phase-noise is -111dBc/Hz at 1kHz offset from the carrier and extends below -133dBc/Hz at far-from-carrier (Fig. 2.20). The oscillation power is -9dBm. This is within the resonator linear operating range. Close-to-carrier phase-noise performance of this oscillator meets the GSM phase-noise specification. To the authors' knowledge, this is the highest frequency micromechanical oscillator reported to-date using a capacitive resonator.

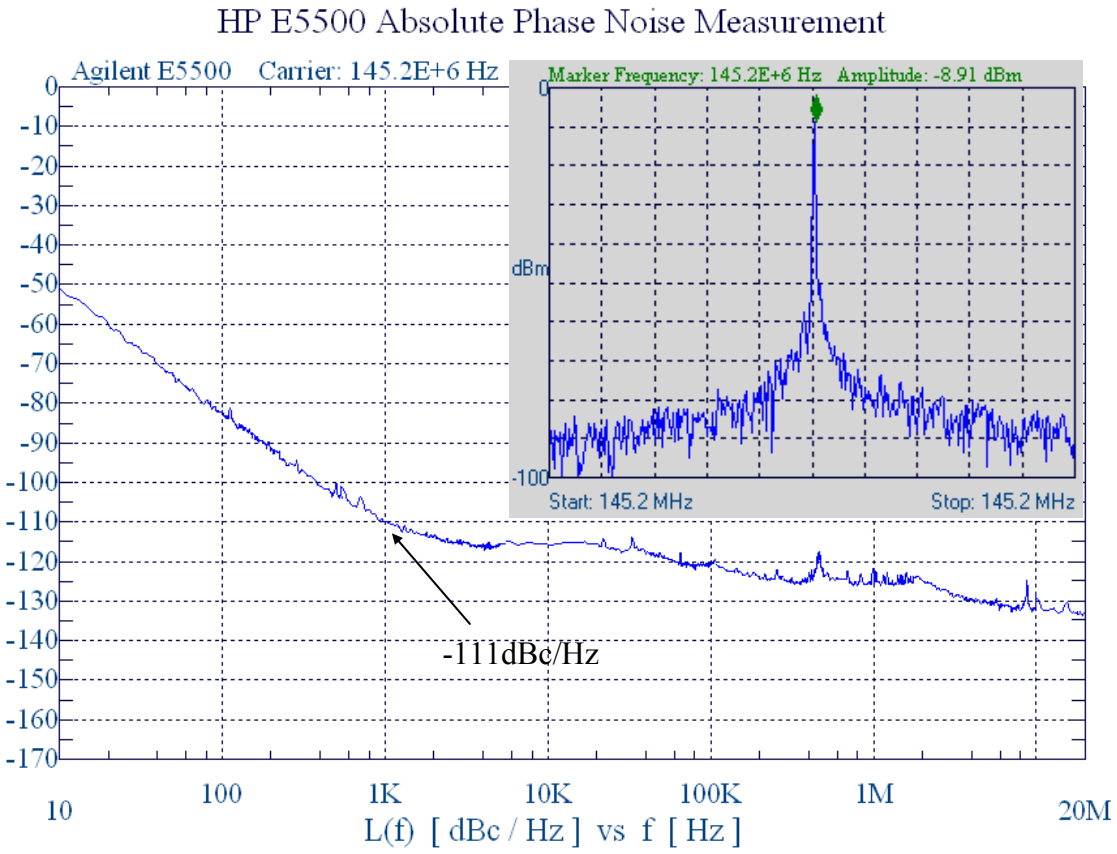


Fig. 2.20. Measured spectrum and phase-noise of the 145MHz oscillator.

2.7.2 High Frequency TPOS Oscillator

As discussed earlier, currently, most reference oscillators are based on quartz crystals. Although quartz oscillators exhibit superior stability and phase-noise performance, their frequency limitation (<200MHz) reduces the performance of multi-mode RF transceivers because of the increase in the up-conversion ratio for the synthesizers.

Prior work on high frequency low phase-noise silicon micromechanical reference oscillators are based on capacitive MEMS resonators with native frequencies in the VHF range [6], [8]. The motional impedance associated with high-frequency (>100MHz) capacitive resonators is usually large (>10kΩ). In addition, capacitive resonator need to

be operated in vacuum and require a DC polarization voltage that is typically beyond what is available in standard IC processes (>5V). This complicates the realization of low-power low-phase-noise UHF oscillators. Laterally-excited TPoS micromechanical resonators, on the other hand, offer an alternative solution as they exhibit significantly lower motional impedances (<1kΩ) at UHF range [20]. In addition, unlike thickness-mode piezoelectric technology (i.e., FBAR), multiple frequency resonators can be integrated on the same substrate.

In this section, a 496MHz reference oscillator based on an AlN-on-Si TPoS resonator is demonstrated [7]. By including silicon in the resonant structure, most of the acoustic energy is stored in a low-acoustic-loss material (single crystal silicon). This boosts the quality factor of the resonator, a key performance parameter for oscillator applications, when compared to a fully piezoelectric resonator (e.g., FBAR).

As shown in Fig. 2.21, the resonator structure resembles a block designed to operate in high order width-extensional resonance mode. The measured motional impedance of the device is ~600Ω and the unloaded Q is ~3800 measured in air. The fabrication process flow of this type of TPoS resonators is low-temperature and post-CMOS-compatible, adding more value to this approach.

The block diagram of the reference oscillator is shown in Fig. 2.21. The frequency of oscillation is determined by either a 496MHz or a 208MHz high-Q TPOS resonator. The sustaining amplifier consists of two parts: TIA with tunable gain and two subsequent

voltage amplifiers. The gain tuning is achieved by a NMOS resistor. The third stage helps relax gain constrains on the previous gain stage; thereby, reducing the power consumption and improving linearity. Due to large power-handling of these resonators (>10dBm), automatic level control (ALC) is not necessary.

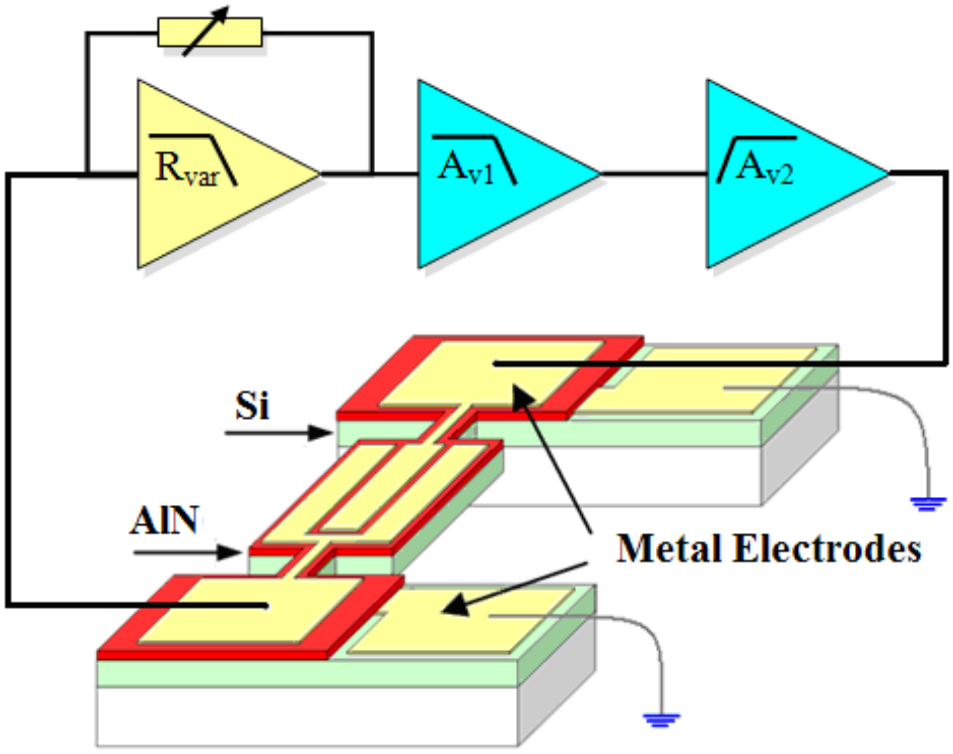


Fig. 2.21. Block diagram of the high frequency TPOS oscillator [7].

The resonators used in this oscillator are 9th-order TPoS lateral bulk acoustic resonator (LBAR) that are fabricated on a SOI substrate with 10µm thick device layer. The finger pitch size is 10µm for 496MHz device and 20 µm for 208MHz device. The frequency is reduced more than 20/10 ratio due to the increase in finger width. The frequency response of the device is measured in air using an Agilent E8364B VNA with GSG probes (Fig. 2.22). Since the termination load of the network analyzer (50Ω) is comparable with the motional impedance of both device (~80Ω and 600Ω) the Q values

measured (~2,520 and ~3,180) are evidently lower than the unloaded Q of the resonator (~7,400 and ~3,800).

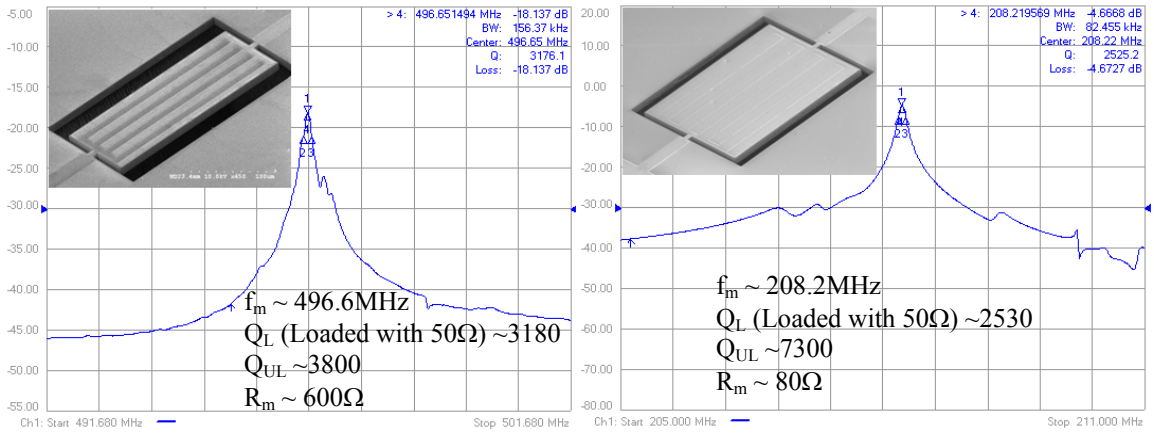


Fig. 2.22. SEM and response of 496MHz and 208MHz AlN-on-Si resonators [7].

The sustaining amplifier is a three-stage 0.18µm CMOS TIA with variable gain at the first stage (Fig. 2.23). The TIA was intended to be a universal design, capable of sustaining oscillation with a broad range of high frequency TPOS resonators having characteristics of: 100MHz < f < 1GHz and 50Ω < R_m < 1kΩ and shunt parasitic capacitance between 1.5pF to 3pF.

To achieve high gain while maintaining the wideband characteristic of the TIA, a low-gain transimpedance stage is followed by two wideband voltage gain stages. Shunt-shunt feedback is introduced in each voltage gain stage to reduce the impedance at inter-stage nodes. This technique increases the frequency of the poles resulting from the inter-stage nodes to much higher than those of the input/output; thus providing wideband characteristic without increasing the power consumption. Another advantage of this technique is to eliminate on-chip inductors typically used in high-gain gigabit CMOS TIA circuits to enhance the bandwidth. The result is significant reduction in area.

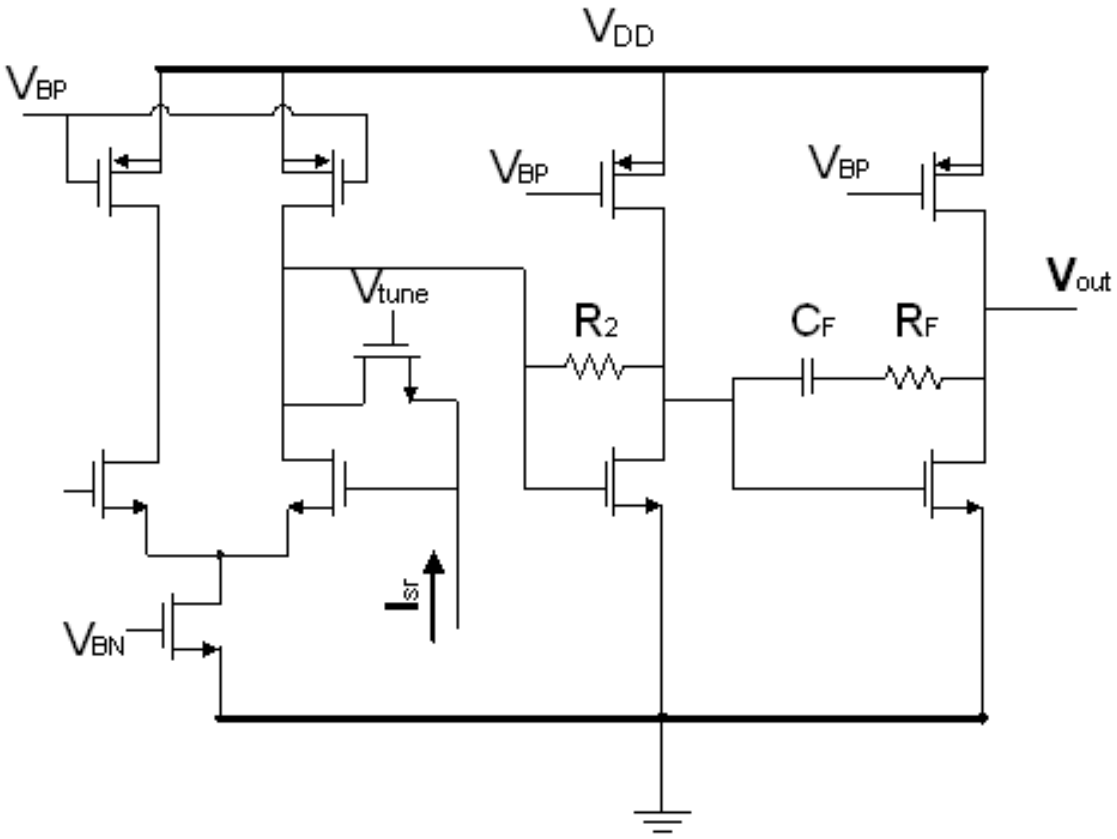


Fig. 2.23. Schematic of the three-stage CMOS TIA (biasing is not shown) [7].

The designed TIA achieves the -3dB bandwidth of more than 880MHz at maximum gain (72dBΩ) when loaded with 2pF capacitance load at the input and output node.

The main reason to choose common source over higher gain topologies such as cascode is to increase the voltage swing and enable the circuit to operate from lower supply (in this case 1.5V) that further reduces the power consumption. The higher output swing results in lower phase-noise floor as the dynamic range of the TIA will be improved.

To boost the gain at higher frequencies, capacitive coupling is used in the third stage. The high pass response of the third stage significantly attenuates the low frequency noise of

the amplifier, which is higher in CMOS circuits due to large flicker noise. Therefore, the contribution of TIA noise to the overall close-to-carrier phase-noise is reduced. The choice of capacitor C_F determines the attenuation. For the case of 2pF, the phase-noise at 1kHz offset is 2dB lower than the oscillator constructed with the same resonator but using the TIA without capacitive coupling.

The TIA and biasing circuitry is fabricated in a 0.18um 1P6M CMOS process. Another TIA that does not incorporate capacitive coupling was also fabricated on the same die for the purpose of performance comparison. An off-chip 50Ω buffer is used to interface with the measurement equipments. The TIA was measured to have maximum transimpedance gain of more than 71.8dBΩ and maximum -3dB bandwidth in excess of 960MHz when loaded with 2pF at both input and output nodes. The TIA -3dB bandwidth when interfaced with standard photodiodes with equivalent capacitance ~500fF will be enhanced to 1.5GHz. The TIA gain could be varied by 8dB (Fig. 2.24). The amplifier and biasing circuitry consumed 6.2mA from 1.5V supply. The die size is $1mm^2$ of which 450μm × 330μm is occupied by the sustaining amplifier (Fig. 2.25).

The measured phase-noise of the oscillator in air is −92dBc/Hz at 1kHz offset and below −147dBc/Hz at far-from-carrier (Fig. 2.26). The measurement was carried out by an Agilent EE5500 phase-noise analyzer. The oscillation power was 1.9dBm, well within the resonator linear range. The slight degradation in phase-noise performance around 100kHz offset is due to the internal phase-noise limit (~−136dBc/Hz) of the Agilent

E8257C Analog Signal Generator that is used in the phase-noise measurement setup. The spurs below 1kHz are caused by 60Hz signal and its harmonics.

To demonstrate the effect of Q loading on the phase-noise of the oscillator, a 208MHz AlN-on-Si resonator that exhibits Q_{UL} ~ 7400 and R_m ~80 Ω was interfaced with the same TIA. The oscillation power was 5dBm. The measured phase-noise at 1kHz offset was −95dBc/Hz and phase-noise floor −152dBc/Hz. While more than 5dB improvement to the phase-noise floor can be explained by the lower motional impedance of the resonator, the less than expected improvement in close-to-carrier phase-noise can be explained by the fact that in both cases, Q_L is roughly the same. Considering R_{in} ~ 100Ω and R_{out} ~ 120Ω, Q_L is 2300 for this device whereas for the case of 496MHz resonator, Q_L is more than 2500. The 3dB difference in phase-noise is due to the fact that the oscillation power for 208MHz is ~3dB higher.

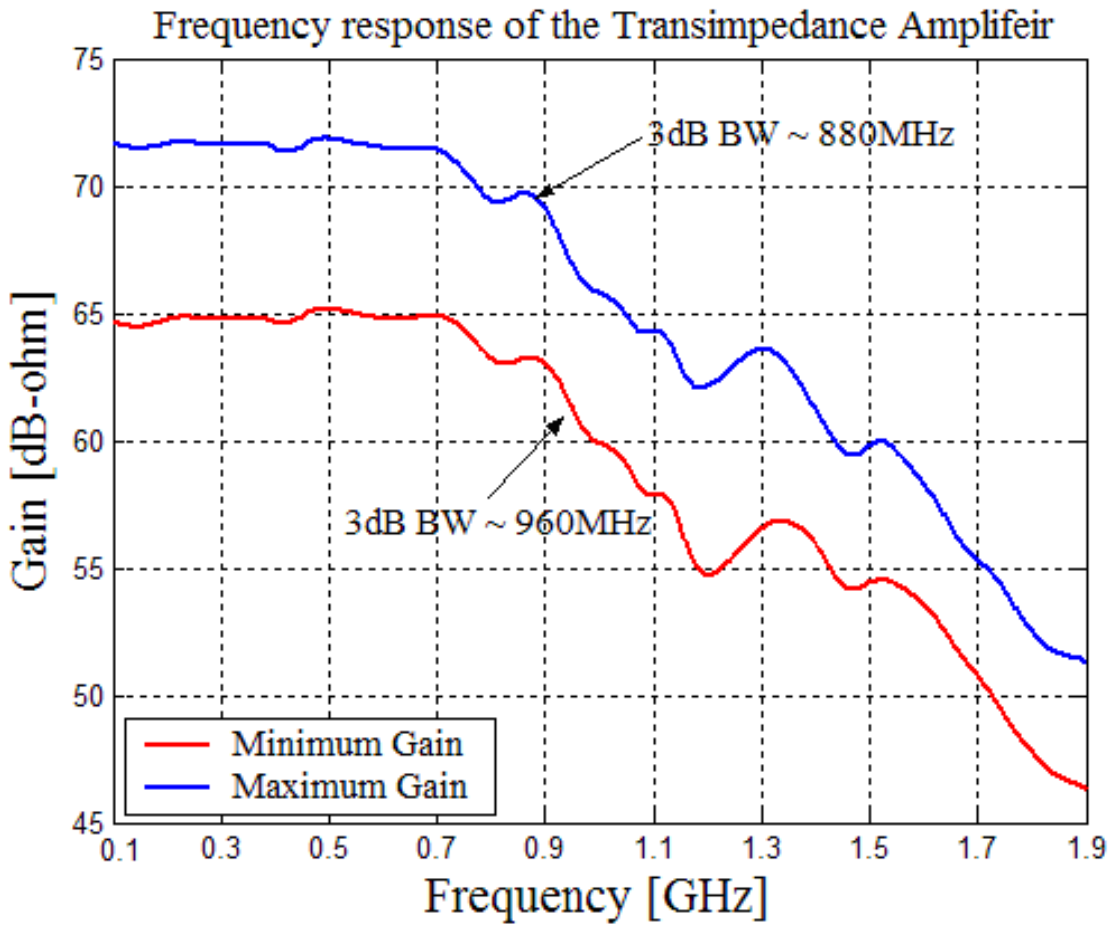


Fig. 2.24. Frequency response of the tunable CMOS TIA [7].

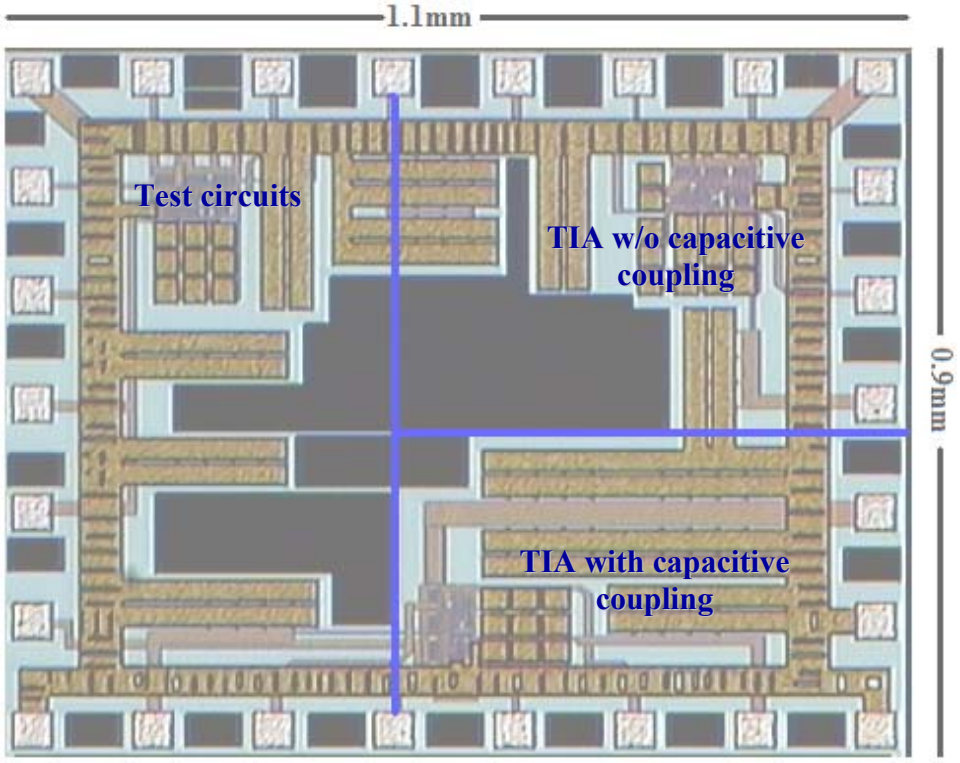


Fig. 2.25. Micrograph of the fabricated die [7].

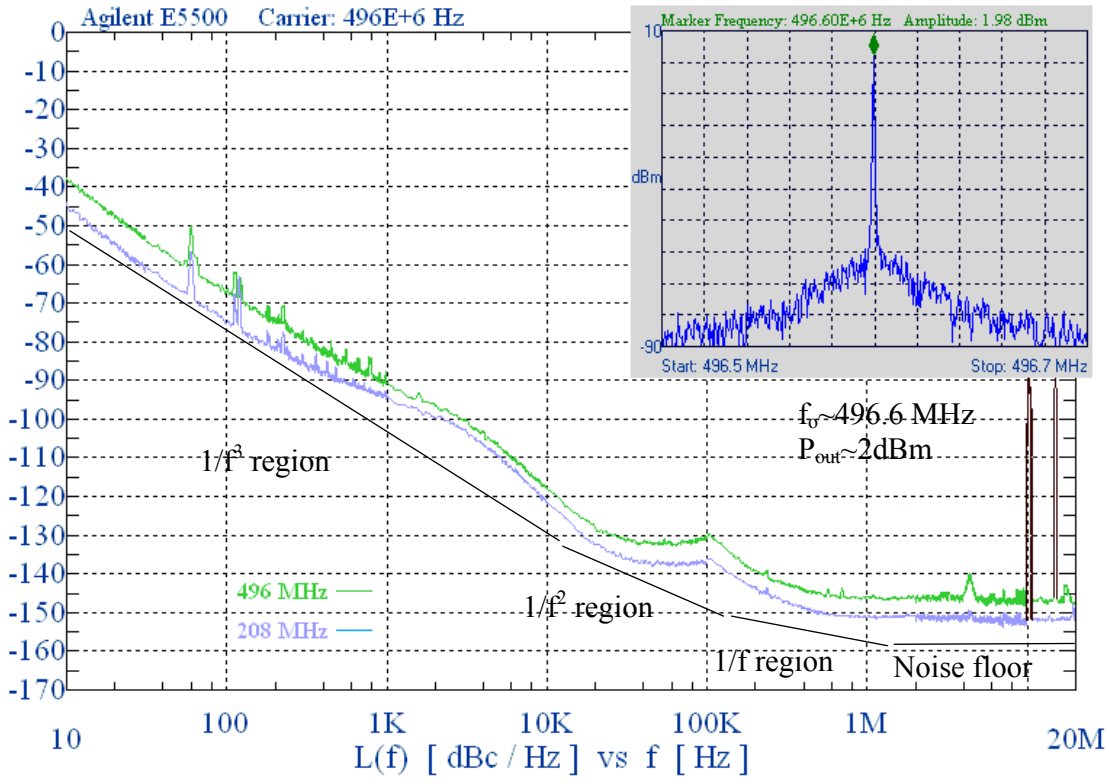


Fig. 2.26. Phase-noise and output spectrum of 208MHz and 496MHz oscillators [7].

The phase-noise performance of the 496MHz AlN-on-Si oscillator, which at the time of publication was the highest frequency lateral micromechanical oscillator, is scaled and compared to state-of-the-art capacitive micromechanical oscillators in Table 2.1.

Table 2.1: Performance comparison of micromechanical oscillators

Oscillator	Disk [8]	SiBAR [6]	This Work		
			61MHz	103MHz	496MHz
PN @ 1kHz (dBc/Hz)	-110	-108	-110	-106	-92
PN @ 10kHz (dBc/Hz)	-128	-120	-136	-132	-118
PN floor (dBc/Hz)	-132	-136	-165	-161	-147
f_m (MHz)	61	103	496		
Resonator Q	48,000	80,000	3,800		
Vacuum	Yes	Yes	No		
DC Voltage	Yes	Yes	No		
IC Process	0.35um	0.18um	0.18um		

2.8 Conclusion

The design of high frequency micromechanical oscillators is explained. The micromechanical oscillator consists of sustaining amplifier and micromechanical resonator. The high frequency lateral resonators that are used in this work are either capacitive SiBAR or lateral TPOS, both of which can be modeled by a series-RLC lumped circuit that incorporates additional shunt and feedthrough capacitance to model non-idealities of the resonator. The sustaining amplifier is usually a tunable TIA that includes a temperature compensation circuit whose output can be applied to the

frequency tuning network for temperature and process compensation. For capacitive resonators with small power handling capability, an ALC can be used to control the oscillation amplitude for best phase-noise performance. Finally examples of high frequency capacitive SiBAR and TPOS oscillators that are realized as part of this work are provided.

CHAPTER 3: Transimpedance Amplifier Design

3.1 Introduction

Due to the high loss of the micromechanical resonator, high frequency MEMS reference oscillators require sustaining amplifiers with large gain bandwidth (GBW). Series-resonant micromechanical resonators call for current to voltage conversion that can be performed in a TIA.

Series-resonant micromechanical resonators typically exhibit large shunt parasitic capacitance at both terminals that directly appear at the input and output of the TIA. This large input/output capacitance load, which is typically a few times bigger than parasitic capacitance of a typical photo-diode (~200-500fF), severely limits the ability of the designer to meet the BW requirements with a reasonable power budget. The design is further complicated by the requirement for high gain and low power consumption. As such, unconventional design methodology may be necessary to deliver a low-power high-gain TIA that is suitable for series-resonant micromechanical oscillators operating in multi-gigahertz frequency range. This chapter describes the TIA design and trade-offs for high-frequency micromechanical oscillators.

At the beginning of this chapter, TIA topologies are introduced and their gain, frequency response and noise performance are compared. After that, the TIA design metrics are explained and trade-offs are briefly explained. The next section focuses on high performance techniques, namely gain and bandwidth enhancement which are critical to improving the TIA performance. Output buffers with large driving capability are

discussed as well. The high performance techniques are then utilized to push the limits of the technology for 0.18μm low-power CMOS TIAs that accompany this chapter as design examples. Finally, different TIA topologies are compared for best performance.

3.2 TIA Configurations

Transimpedance amplifier (TIA) is an active circuit element whose input and output are AC current and voltage, respectively. The transimpedance gain is defined as the ratio of output voltage to input current and is usually expressed in dBΩ. For an ideal TIA, both the input and output impedances are infinitely small and the 3dB bandwidth (BW) is infinitely large. However, in reality, the input and output impedances are finite and tend to move away from pure resistive as the frequency increases. For frequencies well below f_T, the TIA equivalent lumped model can be approximated (Fig. 3.1).

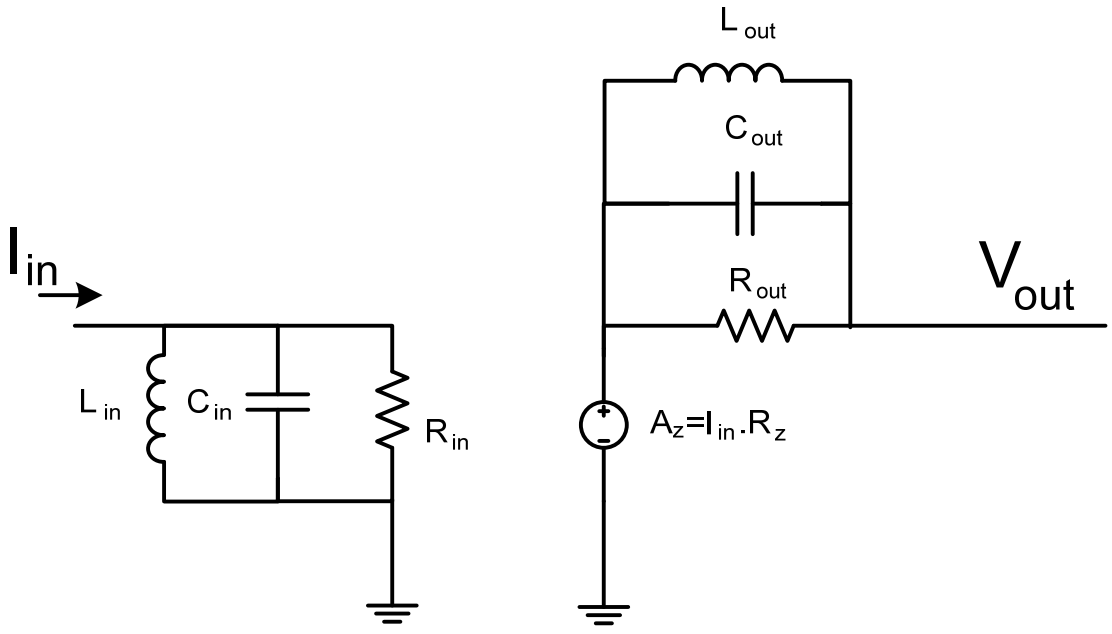


Fig. 3.1. The equivalent lumped model of the TIA

There are two general amplifier configurations that are widely used to realize a current-to-voltage converter amplifier (commonly known as TIA) with large GBW. These topologies are called open-loop and closed-loop (feedback) configurations.

3.2.1 Open-Loop TIA Configuration

The principle of operation in open-loop TIAs is based on a current amplifier with output resistive load. The input current is first amplified by passing through the current amplifier; then, the resulting output current is given to a resistive load to generate an output voltage. Fig. 3.2 shows the concept of open-loop TIA configuration.

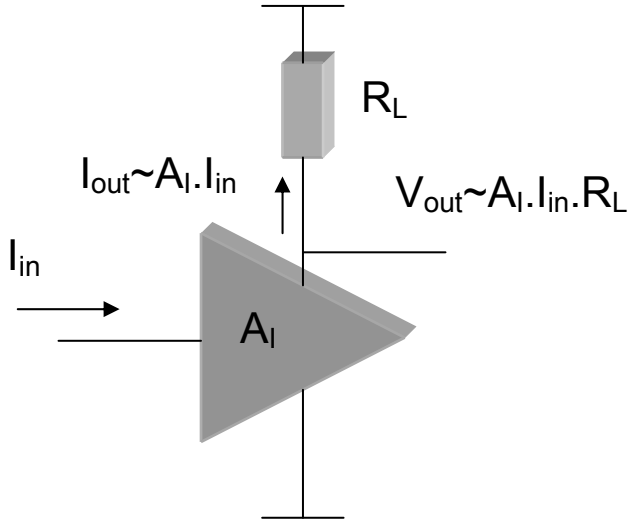


Fig. 3.2. Open-loop TIA concept

The most common amplifier topologies that are used in open-loop TIA configurations are common-gate (CG) and common-base (CB). The inherently-low input resistance of these topologies (~$1/g_m$), makes them ideal for broadband TIA applications. In most cases, the input impedance of the open-loop TIA can be further reduced and consequently the BW can be improved by using boosted-g_m topologies such as regulated-cascade that offers lower input resistance with negligible effect on the gain [59]. Open-loop TIAs are generally lower power but higher noise solutions than feedback TIAs [49].

The high frequency behavior of the open-loop TIA is of extreme importance. Assuming that dominant parasitic capacitance loads are at the input and output of the TIA (this is a reasonable assumption due to the large input and output shunt parasitic capacitance of the micromechanical resonator) and neglecting the channel-length modulation effect ($\lambda \approx 0$ or $r_{ds} \rightarrow \infty$), the frequency response of a CG TIA (Fig. 3.3) can be approximated by:

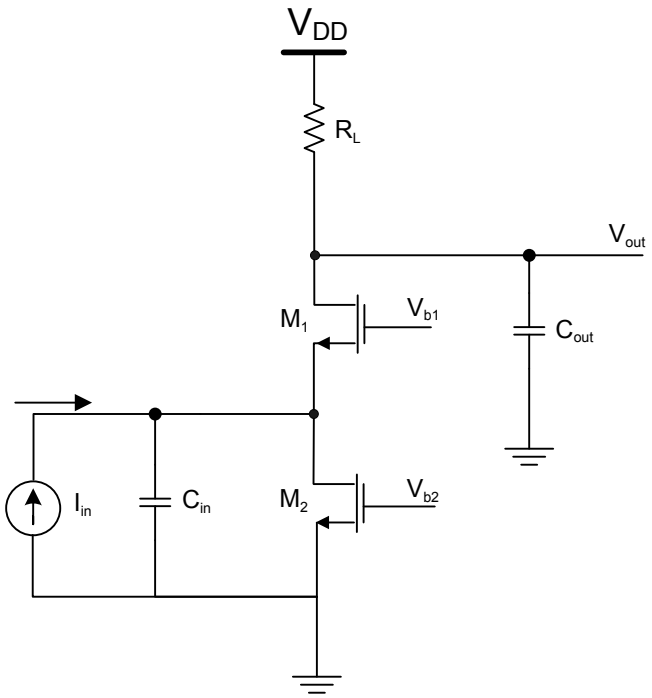


Fig. 3.3. Simplified schematic of a CG TIA

$$\frac{V_{out}}{I_{in}} \approx \left(g_{m1}+g_{mb1}\right).\left(\frac{1}{C_{in}.s}\middle\|\frac{1}{g_{m1}+g_{mb1}}\right).\left(R_D\middle\|\frac{1}{C_{out}.s}\right), \approx \frac{\left(g_{m1}+g_{mb1}\right).R_D}{\left(g_{m1}+g_{mb1}+C_{in}.s\right)\left(R_D.C_{out}.s+1\right)} \tag{3.1}$$

where g_{m1} is the transconductance of M_1 transistor. g_{mb1} is transconductance of M_1 due to the body effect that in short-channel regime, could be as high as $0.4g_{m1}$ for minimum channel length devices. Equation 3.1 clearly shows that the transfer function of the TIA

has two poles. The magnitude of each pole is dependent on the transconductances of M_1 transistor, R_D, and parasitic input and output load capacitances.

Considering the fact that the impedance looking into the source of the M_1 transistor is approximately $1/(g_{m1}+g_{mb1})$, the input impedance of the CG TIA is:

$$R_{in} \approx \left(\frac{1}{C_{in}.s} \left\| \frac{1}{g_{m1} + g_{mb1}} \right. \right). \tag{3.2}$$

Neglecting the channel-length modulation effect on M_1, forces the output current to flow through the parallel equivalent of R_D and C_{out}; therefore, the output impedance of the CG TIA can be approximated by:

$$R_{out} \approx \left(\frac{1}{C_{out}.s} \| R_D \right). \tag{3.3}$$

To realize a low phase-noise micromechanical reference oscillator, it is critical to study the noise behavior of the TIA that is used as sustaining amplifier. Three devices contribute to the output noise of the TIA, two NMOS devices, M_1 and M_2, and the resistors, R_D. Neglecting the gate-induced noise current of MOS devices, the high frequency noise power is mainly due to the thermal noise associated with these three active elements. The equivalent circuit to calculate the input-referred noise current of the TIA is shown in Fig. 3.4. It is worth mentioning that due to the very small BW of micromechanical resonators, spot noise at a particular frequency is a more relevant performance metric than the average noise; as such, computing the total integrated noise in the BW and finding the average noise and noise BW is not necessary. At the first step, it is clear from the equivalent circuit of Fig. 3.4 that the noise of the drain noise current of M_2 directly shows up at the input.

Solving the network for $I_{n,in}$, the equivalent input-referred current noise power can be derived as:

$$\overline{I_{n,in}^2} = \overline{I_{n,M_2}^2} + \frac{C_{in}^2.\omega^2}{\left(g_{m1}+g_{mb1}\right)^2}\overline{I_{n,M_1}^2} + \frac{C_{in}^2.\omega^2+\left(g_{m1}+g_{mb1}\right)^2}{\left(g_{m1}+g_{mb1}\right)^2}\overline{I_{n,R_D}^2}\,, \tag{3.4}$$

where ω is the angular frequency and $I_{n,M1}$, $I_{n,M2}$, and $I_{n,RD}$ are the equivalent thermal noise current of M_1, M_2, and R_D, respectively. The aforementioned noise analysis states that in addition to the thermal noise of the M_2 transistor that directly shows up at the input, the noise of R_D is amplified and referred to the input too. Therefore, CG TIAs are considered an unsuitable solution for low phase-noise micromechanical oscillators.

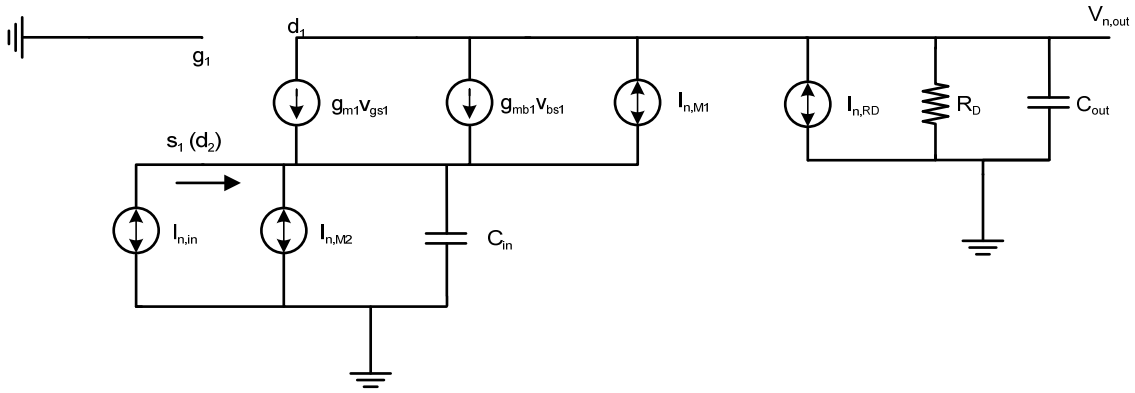


Fig. 3.4. Simplified equivalent circuit for noise calculation in a CG TIA

3.2.2 Feedback TIA Configuration

The feedback TIA configuration is the most common TIA topology used in sustaining amplifiers of lateral micromechanical oscillators due to their low noise and gain vs. BW trade-off flexibility [8], [7]. This configuration is based on a voltage amplifier with shunt-shunt negative feedback between input and output (Fig 3.5). The role of shunt-shunt feedback is to sample the output voltage and return a proportional current to the input of the TIA; effectively acting as the current-to-voltage converter. An important property of

shunt-shunt negative feedback that makes it more attractive for TIA applications is lowering the input and output resistances of the amplifier by loop-gain and naturally, boosting the BW of the TIA. In addition, it helps reduce the equivalent input-referred voltage noise power of the amplifier by the square of the shunt-shunt feedback resistance value. The reduction in noise makes this TIA more attractive for low phase-noise micromechanical oscillators.

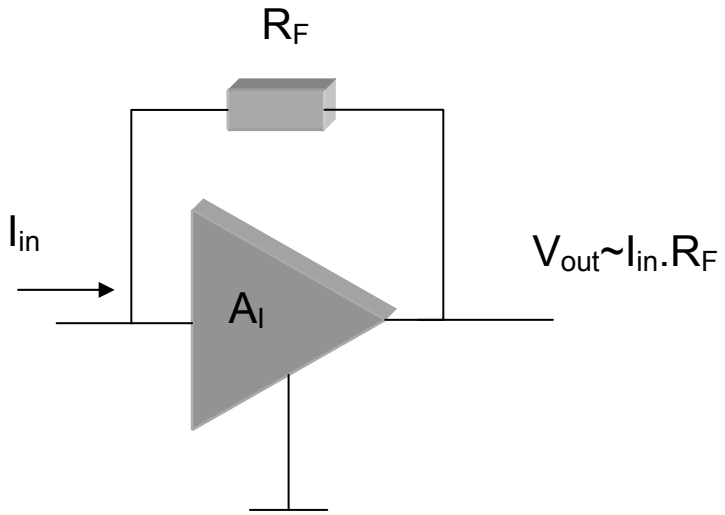


Fig. 3.5. Closed-loop TIA concept

The most common amplifier topologies that are used in feedback TIA configurations are common-source (CS) and common-emitter (CE). Many feedback TIAs are constructed with a single-stage CS amplifier with active load, however, due to the need for larger drive capability and lower output resistance, a source-follower common-drain (CD) stage can be added to the output [49]. Another approach is to use multiple stages each with a shunt-shunt feedback to increase the BW [7].

The frequency response of the feedback TIA shows more flexibility than its open-loop counterpart. It allows for easier trade-off between gain and BW, thereby making the task

of designing a TIA with gain tuning that can be used in micromechanical oscillator applications significantly easier. For a first-order feedback TIA, i.e. the core amplifier is a first-order inverting ideal amplifier with very large input impedance and infinitely-small output impedance, with input and output shunt capacitance (Fig. 3.6), the frequency response can be expressed as:

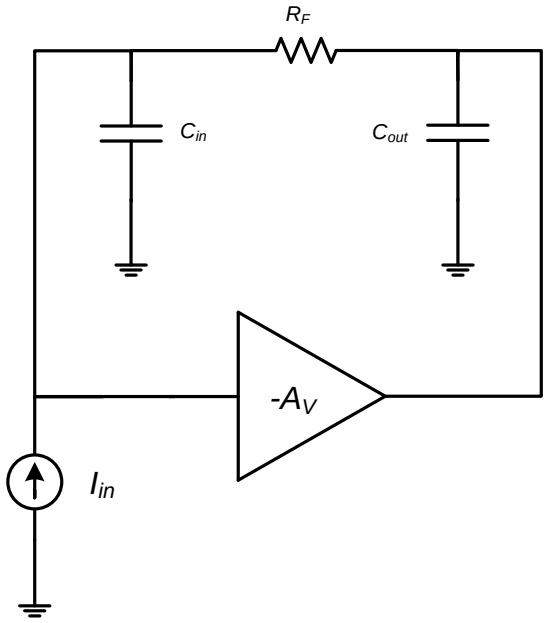


Fig. 3.6. Diagram of the feedback TIA with input and output capacitance load

$$\frac{v_{out}}{i_{in}} = -\frac{A_v}{A_v + 1} \cdot \frac{R_F}{1 + \frac{R_F C_{in}}{A_v + 1} s}, \tag{3.5}$$

where A_v is the open-circuit voltage gain of the core amplifier. The BW of the TIA is limited by the input capacitance and can be traded of by mid-band transimpedance gain, R_F; due to the ideal nature of the voltage amplifier, i.e. the output impedance of the TIA is near zero, the current passing through R_F almost completely flows into the amplifier, leaving only a negligible portion to flow through C_{out}; as such, the output capacitance will

not have a tangible effect on the frequency response of the TIA and hence, can be safely ignored in the AC analysis.

Applying the Miller theorem, the input impedance of the TIA can be approximated by:

$$R_{in} \approx \left(\frac{1}{C_{in}.s} \middle\| \frac{R_F}{1+A_v} \right). \tag{3.6}$$

To study the noise behavior of the first-order feedback TIA, it is imperative to use two-port noise theory to find the equivalent input-referred current and voltages noise sources of the amplifier. Due to the infinitely-large input impedance of an ideal amplifier, the effect of the equivalent input-referred current noise on the noise performance of the TIA is negligible and hence, it can be ignored in the analysis. Fig. 3.7 shows the schematic of the TIA with noise of the core amplifier and feedback resistor. For very amplifiers with very large open-loop voltage gain, i.e. $A_v >> 1$, the equivalent input-referred current noise spectrum of the TIA can be approximated by:

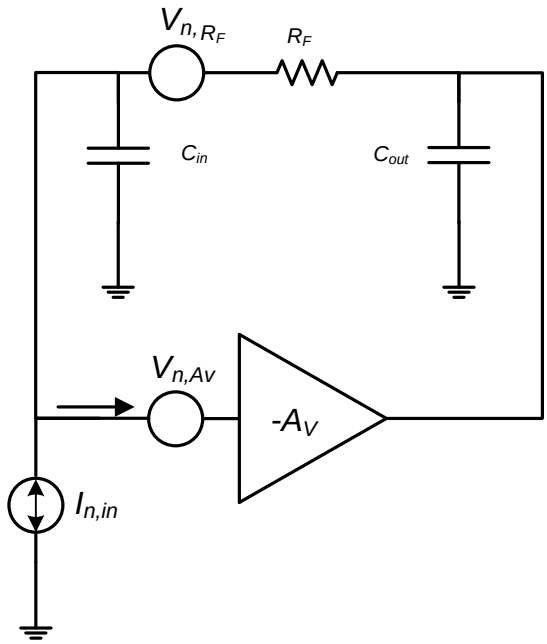


Fig. 3.7. Schematic of the feedback TIA showing the resistor and amplifier noise

$$\overline{I_{n,in}^2} = \frac{\overline{V_{n,R_F}^2} + \left(R_F^2.C_{in}^2.\omega^2 + 1\right)\overline{V_{n,A_v}^2}}{R_F^2}, \tag{3.7}$$

where $V_{n,Av}$ is the equivalent input-referred noise voltage of the core amplifier and $V_{n,RF}$ is the equivalent noise voltage of the shunt-shunt feedback resistor, R_F. The noise expression indicates that at sufficiently-low frequencies, the equivalent input-referred voltage noise of the core amplifier is reduced by a factor equal to R^2_F before showing up at the input of the TIA. This important property of feedback TIAs makes them potentially suitable for low phase-noise micromechanical oscillators where high loss of the high frequency resonator requires a large shunt-shunt feedback resistor which, in turn, helps further reduce the noise of the TIA.

The practical implementation of a feedback TIA in standard IC processes could be a challenge. Although the large impedance looking into the gate of a MOS transistor is considered a reasonably-good emulation of infinitely-large input impedance of an ideal amplifier implemented in CMOS technology, the finite output impedance of a CMOS amplifier combined with the output capacitances limits the BW of the TIA. The resulting TIA can no longer be considered a 1st order system (Fig. 3.8).

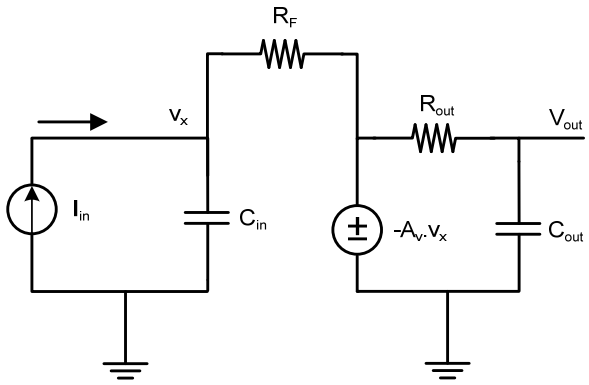


Fig. 3.8. Simplified schematic of the feedback TIA with finite output impedance

The frequency response of the TIA can be obtained by solving the equivalent circuit of Fig. 3.8 for v_{out}:

$$\frac{v_{out}}{i_{in}} = \frac{R_F.(R_{out} - A_v.R_F)}{(R_F.R_{out}.C_{out}.s + R_F + R_{out}).(R_F.C_{in}.s + 1) - (R_{out} - A_v.R_F)}, \tag{3.8}$$

where A_v is the open-loop low-frequency voltage gain and R_{out} is the output impedance of the core amplifier. The equation (3.8) clearly shows that the feedback TIA is now a second order system. The location of the poles is heavily dependent on the feedback resistance, R_F, as well as the input and output capacitance.

The typical implementation of a single-stage CMOS feedback TIA is an inverter with shunt-shunt feedback (Fig. 3.9). A tunable MOS resistor is used to introduce the gain tuning capability in the TIA.

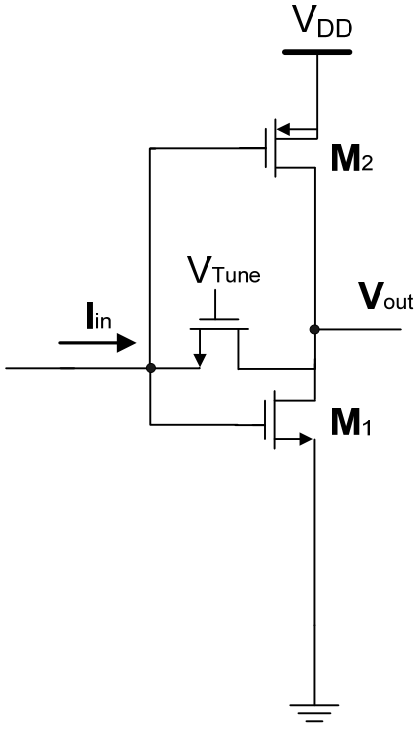


Fig. 3.9. Schematic of single-stage inverter-based tunable feedback TIA

3.3 TIA Performance Metrics for Micromechanical Oscillator Applications

High frequency TIAs used for micromechanical oscillator applications differ from their conventional counterparts that are used in optoelectronics applications by their gain, noise, and BW requirements. Other factors including the power consumption and linearity of the TIA may also have significant impact on the performance of the micromechanical oscillator. This section briefly introduces different TIA performance metrics that are important for micromechanical oscillator applications.

3.3.1 Transimpedance Gain

One of the main obstacles in making high frequency micromechanical oscillators is the high loss of the lateral resonator [12]. This calls for high gain TIA and makes its minimum required transimpedance gain, one of the main criteria for the design of high frequency micromechanical oscillators. High gain comes at a steep price for power consumption and in many cases forces unattractive trade-off with BW [49]. Therefore, gain enhancement techniques may be explored to boost the gain with minimal increase on the power consumption of the TIA.

3.3.2 3-dB Bandwidth (BW)

Perhaps the single most important criterion for the design of TIAs is their minimum BW requirement. To meet the phase requirement for oscillation, the TIA BW should extend well beyond the resonance frequency of the micromechanical resonator. Large shunt parasitic capacitance appearing in most lateral micromechanical oscillators renders many of the conventional bandwidth enhancement techniques inefficient. The stringent power budget allocated to the TIA makes this task enormously-difficult for gigahertz lateral

micromechanical oscillators, as such, special BW and/or combination of several BW enhancement techniques may be considered.

3.3.3 Noise

Low phase-noise micromechanical reference oscillator requires a low noise TIA. Minimizing the noise of the TIA that can be categorized into flicker and thermal noise sources with a given fixed power consumption requires detailed noise analysis and optimization with CAD tools. Optimizing the close-to-carrier phase-noise performance which is a directly affected by the up-conversion of flicker noise, calls for a CMOS TIA with very-low flicker noise. This is markedly different from the conventional TIA design approaches where the only noise source to worry about is the thermal noise

3.3.4 Linearity

The linearity of the TIA has an impact on the integrated jitter of the micromechanical oscillator. This effect is more pronounced on the far-from-carrier performance of the oscillator as the oscillation amplitude is mainly limited by the maximum swing of the TIA which is directly related to its dynamic range. In addition, the total harmonic distortion (THD) of the TIA determines the power of spurious harmonics and sets the overall Spurious-Free Dynamic Range (SFDR). The ever-decreasing supply voltage in advanced CMOS processes puts further strain on the linearity of the TIA and naturally the phase-noise performance of the micromechanical oscillator. This reduced voltage headroom is not particularly troublesome for optoelectronic applications where the output signals are rail-to-rail square wave, however, it should be compensated for low phase-noise micromechanical reference oscillators through linearity enhancement techniques. This could be in the form of adding transistors that operate in triode region, in parallel

with the input device to absorb part of the input power when passing a certain threshold. The devices that operate in triode region are inherently more linear.

3.3.5 Power Consumption

The power consumption is another key factor in the design of the TIA. The overall power budget of the micromechanical reference oscillator imposes a limit on the maximum power consumption of the sustaining amplifier. Stringent gain, BW and linearity requirements of the sustaining amplifier usually do not leave much room for flexibility.

3.3.6 Stability

The stability of an amplifier is an important factor in determining its gain, BW and load driving capability [60]. Although TIAs are inherently designed for stable operation in gigahertz range, some of the gain and BW enhancement techniques negatively affect the stability. While feedback TIAs are relatively immune to instability due to the use of negative shunt-shunt feedback, the excessive GBW that is made available through enhancement techniques, especially pole-cancellation where addition of zero significantly reduces the phase-margin of the amplifier may cause instability. This may show as ringing in the transient response or overshoot in the frequency response [49]. This instability in the oscillation loop may cause the oscillation to build up at another frequency that is totally undesirable. Therefore, stability of the TIA should be monitored across up to the frequency where the transimpedance gain is larger than unity, i.e. unity gain-bandwidth (UGBW). One approach to reduce the instability caused by excessive gain or large capacitance load is to use a feedthrough capacitance between the input and output of the TIA. This feedthrough capacitance controls the overshoot by introducing a zero in the transfer function of the TIA at the expense of smaller BW.

3.4 High Performance Techniques

The need for a high gain TIA that is capable of tolerating large parasitic capacitance is explained in previous section. The focus of this section is on ways to improve the TIA performance with minimal impact on its noise performance and power consumption. The main performance criteria that need immediate attention are gain and BW of the TIA.

3.4.1 Gain Enhancement

There are several low-power gain enhancement techniques that can be used in conjunction with other high performance techniques to deliver a low-power high-gain broadband CMOS TIA suitable for high frequency micromechanical oscillators. Most of these techniques are programmable and can be used with both open-loop and feedback TIAs in lateral micromechanical oscillators.

- Auxiliary load:

To circumvent the constraint imposed by limited supply voltage in advanced CMOS processes, it is possible to add a PMOS (or NMOS) load in parallel with the drain resistance, R_D, of the CS or CG amplifiers (Fig. 3.10) [49]. This MOS device is biased such that a portion of the drain current is supplied by this transistor. Since the output impedance of a current source made of a MOS transistor is significantly higher than the drain resistance used for high frequency TIAs, it is possible to increase the overall transimpedance gain. Careful balance between the current of the MOS current source and the drain resistance ensures appropriate gain with minimal impact on the BW of the amplifier. The main disadvantages of this gain enhancement method are the increase in the total noise and reduced linearity.

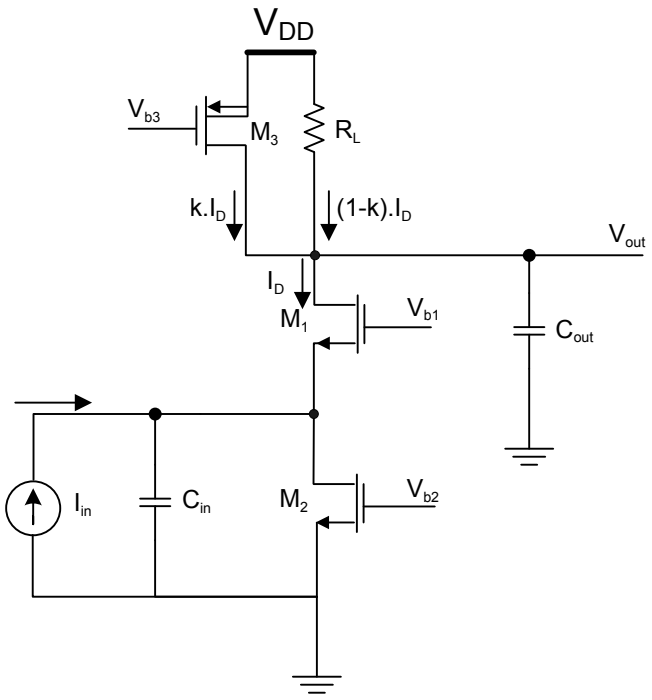


Fig. 3.10. Schematic of CG TIA with auxiliary PMOS load

- Cascode:

A popular approach to increase the gain of an amplifier is cascoding. The gain boosting is achieved through increase in the output resistance of the amplifier. The cascode device will appear as CG for the input signal, effectively providing additional amplification before the signal is arrived at the output. Assuming that the MOS devices are identical and exhibit sufficiently-large drain-source resistance, the gain improvement can be approximated by:

$$\frac{A_{v\_boosted}}{A_v} \approx r_{ds}, \tag{3.9}$$

where r_{ds} is the drain-source resistance of the MOS device. While for open-loop TIAs, the amount gain improvement is roughly equal to that of a simple voltage amplifier, the gain of the feedback TIA does not improve much as it is primarily determined by the value of the feedback resistor.

With high demand for high frequency low phase-noise reference oscillator based on capacitive micromechanical resonators, the gain improvement due to the use of a cascode topology may not be sufficient. Increasing the number of cascode devices to two, i.e. triple-cascode topologies is considered an option; but it comes at the expense of further reduction in voltage headroom that can only be tolerated in higher voltage older generation CMOS processes (>3V). A more practical approach is based on "boosted" or "regulated cascode" (RGC) topology where the output resistance can be increased substantially by the gain of the feedback amplifier [60] (Fig. 3.11). The feedback amplifier can be a simple CS with active load.

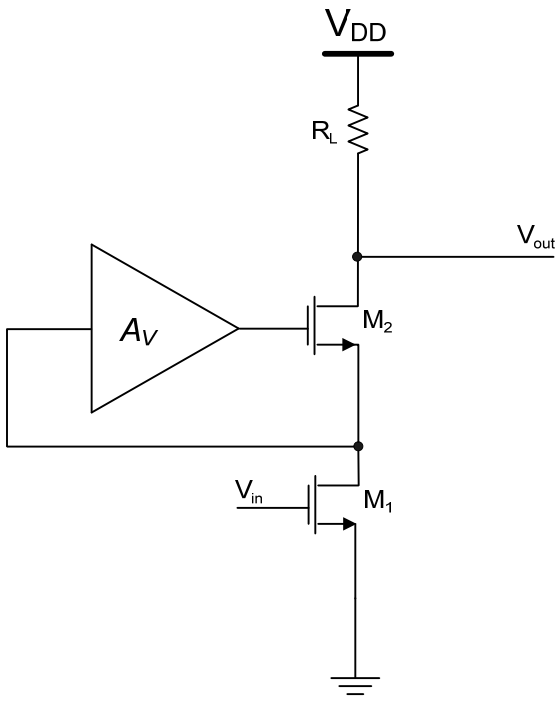


Fig. 3.11. Simplified schematic of amplifier with boosted cascode load

- Cascade of amplifiers:

The most effective approach to reliably increase the gain of an amplifier in advanced CMOS processes is through the cascade of two or more lower gain amplifiers. The total

gain will be the product of the gain of amplifiers (Fig. 3.12). For practical reasons, this technique is usually applied to several single-stage amplifiers with low gain and large BW. For TIA applications, the first stage is normally a transimpedance stage; subsequent stages are voltage amplifiers that boost the signal level in voltage domain. Cascaded amplifiers will have the potential for lower instability threshold. This is usually due to the extra poles in the transfer function of the amplifier that significantly reduce the phase-margin. Since any compensation technique will shrink the BW of the amplifier, the designers usually opt for lower gain stages with feedback that can push the poles to higher frequency and hence, reduce their impact on the phase of response of the cascaded amplifier. Famous approaches include cherry-hooper amplifiers that can offer large GBW with acceptable stability [49].

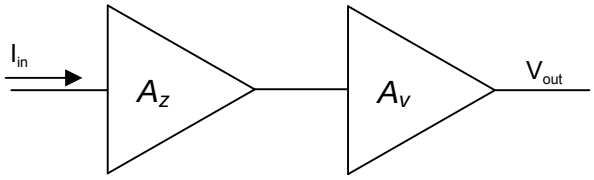


Fig. 3.12. Block diagram of the cascaded TIA

- Current amplification:

Since the input to the TIA is current, it may be worth to consider boosting the signal in the current domain and then pass it to the transimpedance stage for current-to-voltage conversion. This approach is conceivable only if the current amplifier is sufficiently low power and its BW is comparable (and preferably beyond) with the required BW of the TIA (Fig. 3.13). A simple broadband current amplifier is MOS current mirror with 1:N ratio (N>1). This ratio should be carefully chosen to avoid unreasonable increase in the power consumption of the TIA.

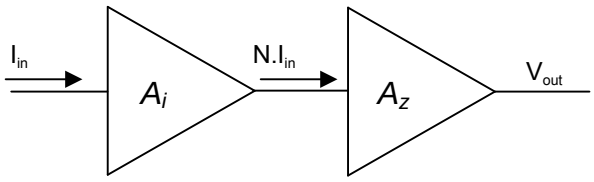


Fig. 3.13. Block diagram of the TIA w/ current pre-amplification for gain boosting

3.4.2 BW Enhancement

To address the BW reduction caused by large parasitic capacitance of high frequency lateral micromechanical resonators, novel low-power BW enhancement techniques are necessary. These techniques fit into one of these two sub-groups:

✓ Pushing the transfer function poles to higher frequency:

In this category, the BW extension is realized by reducing the impedance to ground at critical nodes. This reduction helps push the poles to higher frequency and naturally, increase the BW of the TIA. Prime example of this approach is to use shunt-shunt feedback in the TIA.

- Feedback:

Study of feedback theory reveals that shunt-shunt feedback have a positively effect the BW of the TIA through reducing the input and output impedance of the closed-loop feedback system by a factor close to the loop gain of the system [60]. Considering the large shunt parasitic capacitance of the lateral micromechanical resonator, the feedback pushes the poles to much higher frequency and hence, greatly improves the BW of the TIA. In many cases, however, the BW limitation due to inter-stage poles is a bigger problem that weights over the design methodology. Here, the first stage acts as the current-to-voltage conversion stage while local shunt-shunt feedback resistor incorporated into other stages lower the equivalent impedance seen at each critical inter-

stage node (Fig. 3.14). Of course, adding additional feedback resistors in each stage hampers the goal of making a high-gain low-power TIA. A Cherry-Hooper topology that minimizes the use of feedback resistors can be considered as a compromise [49]. For any given two-stage amplifier that uses local shunt-shunt feedback in each stage, the feedback in the first stage can be eliminated in favor of higher gain. In this case, the shunt-shunt feedback in each stage lowers the equivalent resistance at both terminals by loop-gain, therefore, in N-stage amplifiers (N>=3), the shunt-shunt feedback in the even stages (2, 4, etc) will be redundant (Fig. 3.15). The main disadvantage of cherry-Hooper amplifiers when used in micromechanical oscillator applications is their reduced stability and minimal control over the large signal behavior of the amplifier. For very-high gain applications (>80dBΩ), it is recommended to keep in the shunt-shunt feedback in each stage for improved level control and immunity to process and temperature variation.

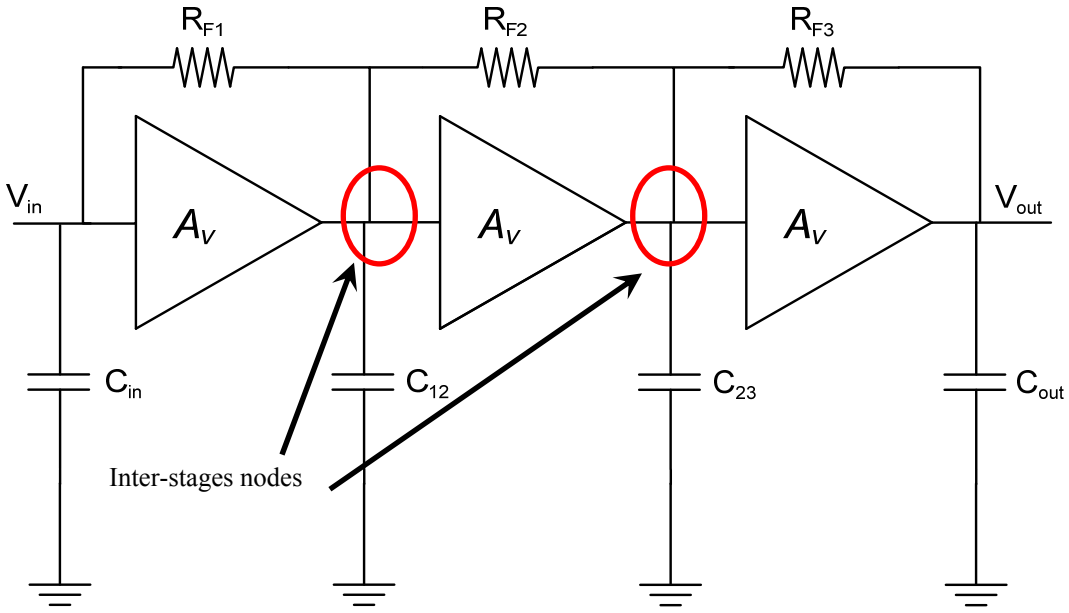


Fig. 3.14. Diagram of a multiple-stage amplifier with local shut-shunt feedback

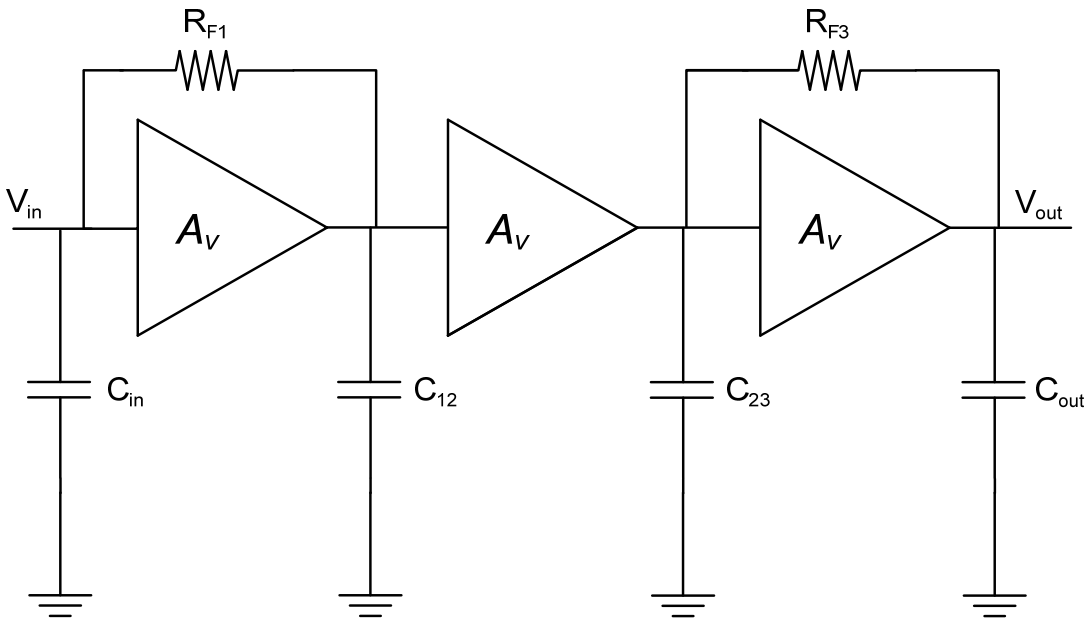


Fig. 3.15. Diagram of a multiple-stage amplifier that shows Cherry-Hooper concept

- Low-impedance input and output stages

Even after addressing the problem with inter-stage poles, large parasitic capacitance of lateral micromechanical resonators continue to pose serious challenges at the input and output of the TIA. While permanent solution to this problem usually lies in the design of resonators with smaller shunt parasitic capacitance, using low-impedance input and output stages can reduce the intensity of the problem.

Most low-impedance input stages take advantage of $1/g_m$ concept; i.e. the input impedance is proportional to the inherently-small $1/g_m$ of the input transistor. CG topology is the most famous example in this class. Another example is a diode-connected current-mirror amplifier that is combined with current-to-voltage conversion stage. In some cases, excessively-large shunt parasitic capacitance requires further reduction in

input impedance. A known method is to use boosted-g_m that is commonly known as regulated cascode topology (RGC) (Fig. 3.16).

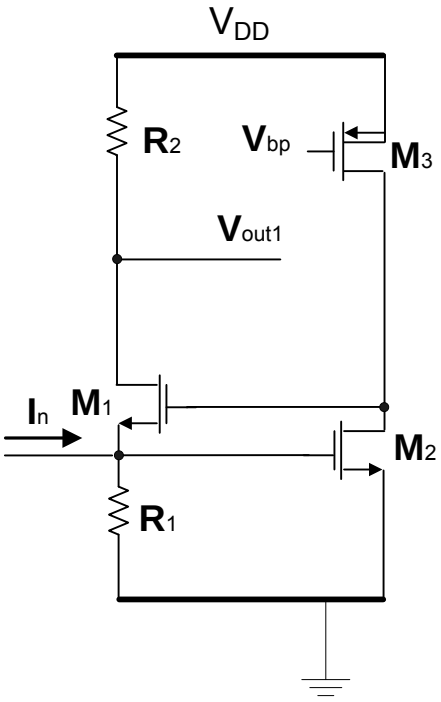


Fig. 3.16. Schematic of an RGC TIA

For RGC TIA shown in Fig. 3.16, the input impedance can be expressed by:

$$R_{in} = \frac{1}{g_{m1}(1 + R_1.g_{m2})}, \tag{3.10}$$

where g_{m1}, g_{m2}, and R_1 are transconductance of M_1, M_2, and load resistance in g_m-boosting amplifier, respectively. As mentioned in the previous section, any type of CG-based topology suffers from high input-referred noise and hence, is not suitable for ultra-low phase-noise micromechanical oscillator applications.

For micromechanical oscillator applications, lowering the output impedance of the TIA is equally important. A well-known low-impedance output stage is common-drain (CD) stage that is otherwise known as source follower. The output impedance of this stage is

proportional to $1/g_m$ of the transistor. Further reduction in output impedance can be achieved by introducing a feedback in source-follower stage. The feedback helps reduce the output impedance by a factor close to the loop-gain of the closed-loop system. This topology is sometimes called super source-follower [61]. Poor linearity and limited dynamic range are among the well-known problems of source-follower topology.

- Introduce zeros in the transfer function to cancel the effect of poles:

This approach relies on the pole-zero cancellation concept for BW enhancement; one or more zeros are introduced in the transfer function of the TIA. The locations of these zeros are precisely determined to cancel the effect of poles (especially the dominant pole). The famous examples of this approach are series and shunt inductive peaking.

- Pole cancellation (inductive peaking and capacitive degeneration)

The BW improvement in this method can be explained by introducing one or more left-hand plane zeros in the transfer function whose frequency can be varied accurately to match those of one or more poles in the transfer function. The concept relies on the added positive phase-shift from the zero to compensate for the negative phase-shift that is caused by the pole. The left-hand zeros do not cause the system to become unstable. Although pole cancellation is a very popular approach to increase the BW for very-high frequency TIAs (BW>10GHz), it has been neglected to some extent for lower frequency TIAs with cut-off frequency in upper UHF range (1GHz<BW<3GHz). This is mainly due to the large size of on-chip monolithic inductors (>10nH) that are required to realize left-hand plane zeros for TIA operating in this range. A solution to this problem is to replace passive inductors with active inductors [49], [62]. Not only active inductors are smaller,

they are tunable and can be designed to have higher Q. The main drawbacks of active inductors are high noise associated with active components and poor linearity.

There are two major approaches to introduce zeros in the transfer function: series peaking and shunt peaking. The concept of series peaking is based on putting a circuit element in series with the input or output of the TIA to create a zero in the transfer function. In rare cases, it is possible to place this element between two stages [63]. Shunt peaking follows a similar approach with the exception that this element is placed in parallel with the input and/or output of the TIA. In majority of the cases, this extra element is an inductor (passive or active). For series-peaking, the inductor is usually placed at the input to resonate out the input pole while for the shunt-peaking, the inductor is intended to resonate out the output pole and hence appear in shunt with the output of the TIA. Fig. 3.17 shows the concept of peaking for amplifiers.

There are other methods to create a zero in the transfer function of the TIA. Placing a feedthrough inductor between the input and output of the TIA is a well-practiced approach for BW enhancement through creating an additional zero, however, due to practical reasons, this approach is only suitable for wideband amplifiers (BW>10GHz).

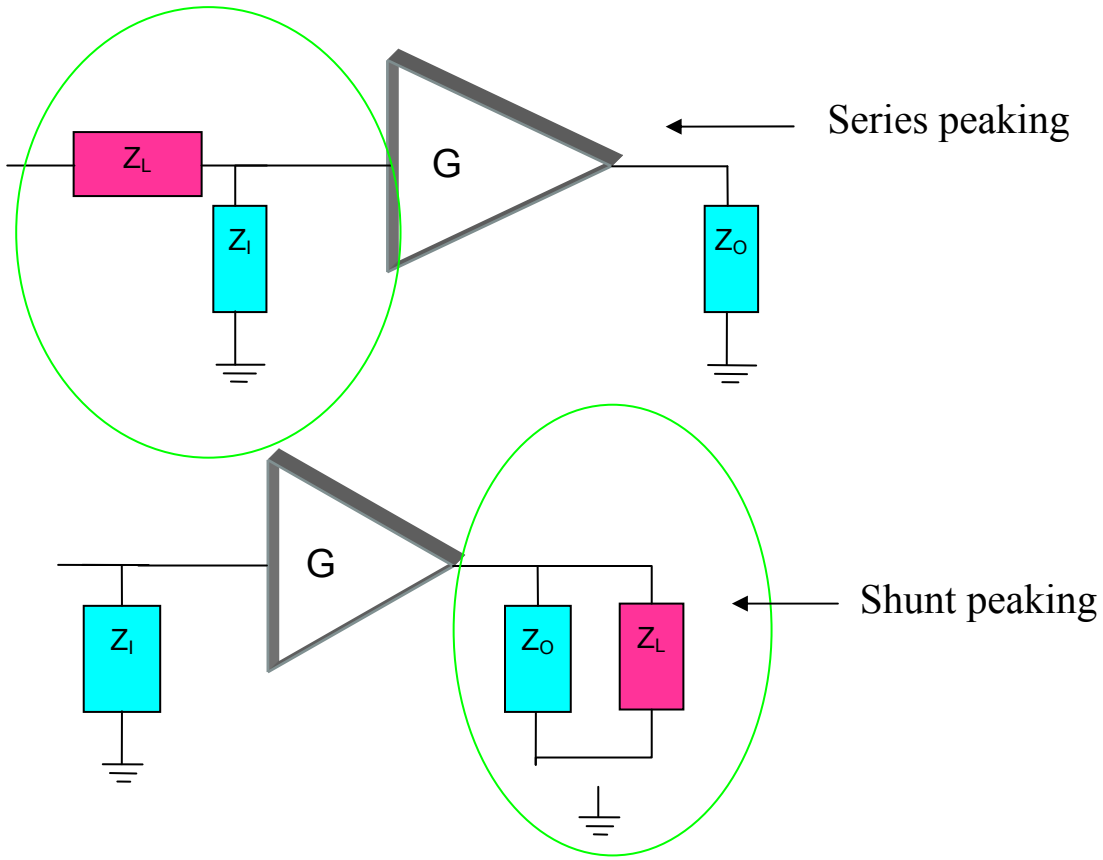


Fig. 3.17. Block diagram of TIA showing both series- and shunt-peaking concept

Capacitive coupling is another pole-cancellation BW enhancement method that can benefit TIAs interfaced with micromechanical resonators. This approach is attractive for high gain lower BW (f<1GHz) micromechanical oscillator applications where the value of inductors that can be potentially used for inductive peaking is significantly larger than what can be practically realized on chip (Fig. 3.18). The output pole resulting from the equivalent output resistance and the capacitance load can be resonated out by the zero that is generated by source degeneration resistor and the extra capacitance to the reference ground. This results in boosting G_m off the amplifier at higher frequencies.

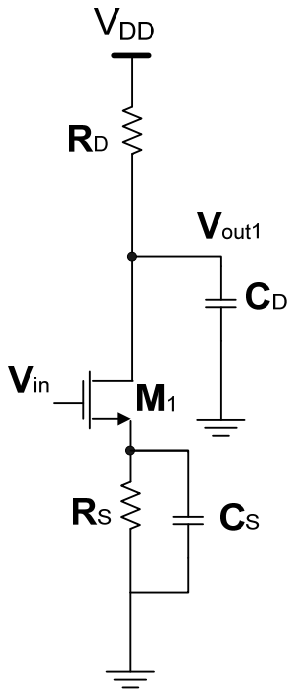


Fig. 3.18. Schematic of an amplifier with capacitive coupling for BW enhancement

- Other techniques:

There are several less popular techniques that can be used to increase the BW of a TIA with limited effectiveness for micromechanical oscillator applications. For example, f_T-doubler topologies [64] are designed to reduce the effective parasitic capacitance of the input transistor (usually C_{GS}) by 50%. This could theoretically increase f_T by 2× and potentially increase the BW. But this approach is only applicable to TIAs whose BW is limited by parasitic capacitance of the transistor itself. However, this approach is clearly not applicable for lateral micromechanical oscillators where the shunt parasitic capacitance of the resonator sets the dominant pole. In addition f_T-doubler adds to noise.

3.5 Output Buffer

Buffers are needed to drive large loads that appear the output of micromechanical oscillators. These loads are either in the form of a large equivalent capacitance of

subsequent blocks in the frequency synthesizer, or for stand-alone oscillators, is in the form of a small resistance (usually 50Ω input impedance of the line) combined with the parasitic inductance and capacitance of package and interconnects. This section identifies several CMOS output buffer topologies that are suitable for micromechanical oscillator applications and briefly lays out the design procedure for each topology.

3.5.1 Inverter Topology

One of the famous buffer topologies that are used to drive large capacitance load is the inverter topology. The inverter buffer is a relatively low-power topology offers large driving capability with rail-to-rail output in compact size. Its very-high output impedance obviates the need for an impedance matching network for high-speed signals. However, this high-impedance approach is only acceptable where the parasitic from interconnects between the inverter and the capacitance load is very small (Fig. 3.19). This is usually the case when the inverter is used as an output buffer for on-chip micromechanical reference oscillator used in a frequency synthesizer. In this case, the frequency synthesizer blocks are laid out very close to each other and therefore, the interconnect parasitics are negligible. For off-chip capacitors, this approach has a potential drawback; the reflection caused by mismatch between characteristic impedance of the line and the high output impedance of the inverter gives rise to severe distortion in the amplitude and phase of the signal which directly shows up in the phase-noise performance. In this case, a simple matched line can do the job.

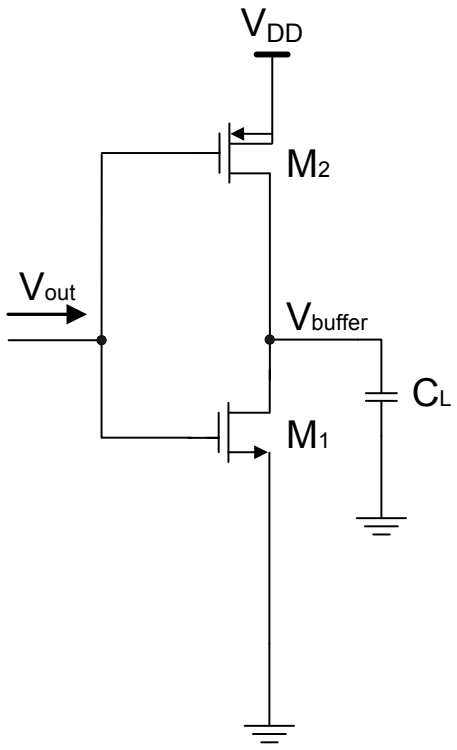


Fig. 3.19. Schematic of inverter buffer with capacitive load

The maximum speed of the inverter can be approximated by finding the rise time and fall time. Then, the minimum acceptable period for a signal can be found by averaging the rise and fall times. This is called the propagation delay of the inverter:

$$t_p\big|_{HL} = \frac{C_L V_{DD}}{K_n\left(V_{DD} - V_{T,n}\right)^2}, \tag{3.11}$$

$$t_p\big|_{LH} = \frac{C_L V_{DD}}{K_p\left(V_{DD} - \left|V_{T,p}\right|\right)^2}, \tag{3.12}$$

$$t_{p,avg} = \frac{t_p\big|_{LH} + t_p\big|_{HL}}{2}, \tag{3.13}$$

where C_L is the load capacitance, $V_{T,n}$ and $V_{T,p}$ are the threshold voltages for N-type and P-type MOS device, and K_n and K_p are K factors for N-type and P-type devices, respectively.

3.5.2 Doubly-Terminated (50Ω-Matched) Topology

The best approach to deliver a large signal to output load with minimum loss is to use a load-matched buffer. The load impedance is usually near-50Ω with negligible reactive component. A prime example is the 50Ω input impedance of RF measurement equipments. In an unlikely case that the load impedance and the line characteristic impedance are different, the buffer output should be matched to line. Alternatively, a transmission line impedance transformer can be used to perform proper matching.

The simplest CMOS topology for 50Ω buffer is a CS with near 50Ω resistive load. The load resistance has to be carefully adjusted to account for the equivalent output resistance if the MOS transistor, which for high-speed high-power buffers, could be comparable to the impedance of the load. For very high frequency applications where parasitic capacitance of the MOS device is not negligible, an on-chip inductor is placed in series with the load resistor to resonate out the unwanted pole (similar to shunt peaking). This inductor is usually chosen as a passive monolithic inductor for best linearity and noise performance. Fig. 3.20 shows a simplified schematic of a 50Ω-matched buffer with inductive shunt peaking.

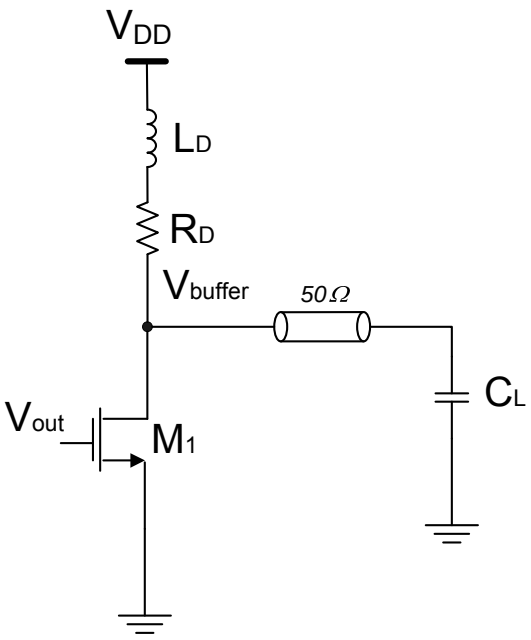


Fig. 3.20. Simplified schematic of a 50Ω-matched output buffer

3.5.3 Open-Drain Topology

Open-drain output topology is the most popular output topology for high-speed optoelectronics system as it can produce large output swing for far-end when the load is matched to the characteristic impedance of the line.

This output buffer topology is mostly used in differential configuration to minimize noise coupling from nearby high-speed lines and supply lines all of which appear as common-mode to the differential buffer and hence, are substantially attenuated. Stability of the buffer is improved as well; however, it still remains an issue especially instability due to feedthrough parasitic impedances. The only outstanding problem with differential operation is the increased power consumption that may be a concern for on-chip systems.

For near-end applications such as on-chip buffering, the buffer exhibits high output impedance and makes it unattractive for most micromechanical oscillator applications. As such, the design methodology for the open-drain buffer is not explained here.

3.6 Design Examples

The knowledge acquired during the previous sections is utilized to design and characterize several low-power high-gain CMOS tunable TIAs. This section details the design procedure, measured performance, and interface data with micromechanical resonators for each of these TIA.

3.6.1 Regulated Cascode TIA

This CMOS TIA is intended for low-power applications, therefore, an open-loop configuration is chosen. In this approach, a non-inverting RGC current-to-voltage conversion stage is cascaded with a tunable inverting voltage amplification stage in which the input and output signals are out-of-phase (Fig. 3.21). Outputs from both inverting and on-inverting stages are taken out to enable operation with both in-phase and out-of-phase micromechanical resonators [65]. When operating in non-inverting mode, the second stage is bypassed and the output is taken from the first stage. In inverting mode, the second stage provides additional 180º of phase-shift.

To drive a resonator with large parasitic shunt capacitance (C_P~2pF) into oscillation, both input and output resistance of the sustaining amplifier have to be reduced such that the resulting poles are pushed to frequencies much higher than the oscillation frequency. To achieve this, a gm-boosted common-gate topology, commonly-known as regulated cascade (RGC) is used for the first stage [59]. The input resistance of the TIA further

reduced by the loop gain of the feedback system; therefore, increasing the g_m of both transistors helps reduce the input resistance:

$$R_{in} = \frac{1}{g_{m1}(1 + R_1 . g_{m2})}, \tag{3.14}$$

where g_{m1}, g_{m2}, and R_1 are transconductance of M_1, M_2, and load resistance in g_m-boosting amplifier, respectively.

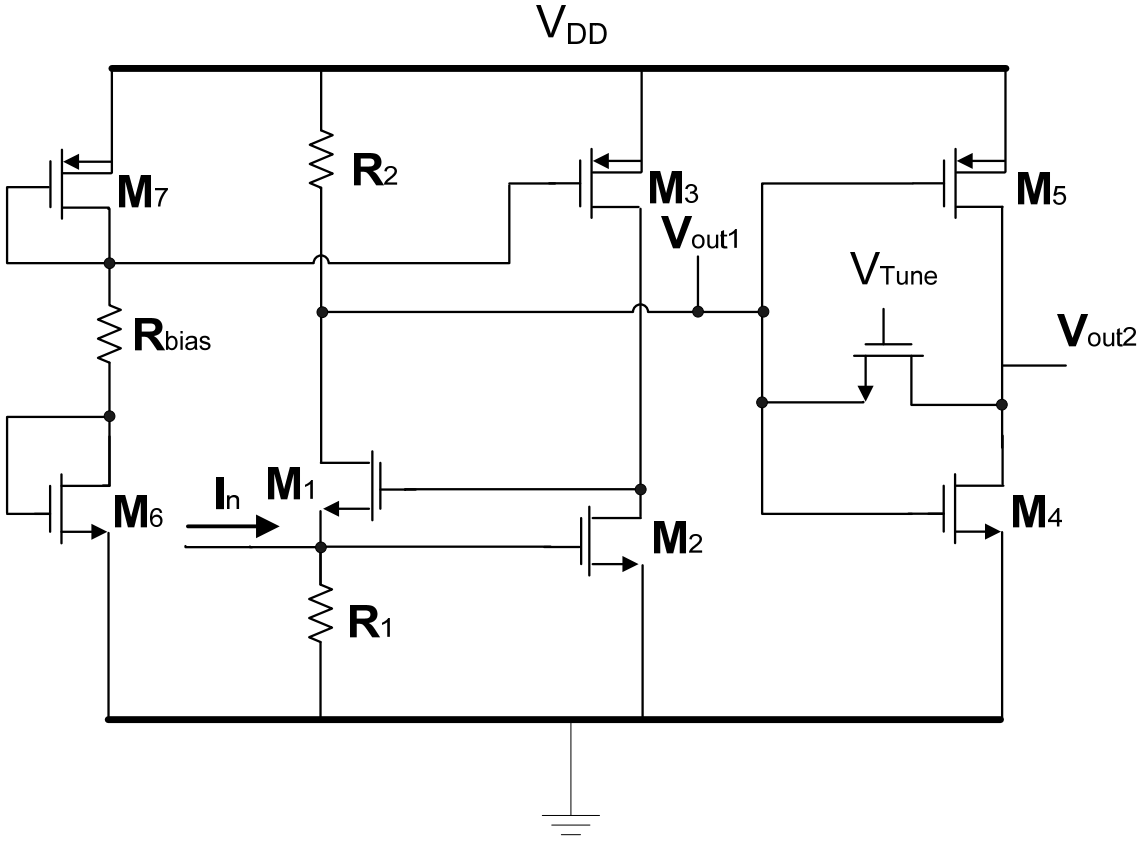


Fig. 3.21. Schematic of the two-stage RGC TIA

The transimpedance gain is mainly set by the gain of the RGC stage. The gain of this stage is traded-off with lower output impedance to avoid creating a high-impedance node, and consequently a low-frequency pole, that may limit the BW of the TIA when driving the large shunt parasitic capacitance of the resonator in non-inverting mode.

The second stage is an inverter with tunable shunt-shunt resistive feedback. The choice of inverter over CS is made due to the availability of higher voltage gain with the same power consumption. The overall transimpedance gain when both NMOS and PMOS transistors are operating in saturation is:

$$R_{CL,RGC} \approx \left(R_2 \| R_{tune}\right).A_{v2}\,, \tag{3.15}$$

where R_{tune} and A_{v2} are the shunt-shunt feedback resistor and voltage gain of the second stage, respectively. The shunt-shunt feedback is used to reduce the output impedance, hence, making the second stage capable of driving large shunt-parasitic capacitance without the need for additional buffering. The shunt-shunt feedback resistance, R_{tune}, is realized by a NMOS device, M_5, which operates in linear region. The voltage gain of the second stage can be approximated by:

$$A_{v2} \approx -\left(g_{m1} + g_{m2}\right).\left(r_{o1} \| r_{o2} \| R_{tune}\right), \tag{3.16}$$

where g_{m1} and g_{m2} are transconductance, and r_{o1} and r_{o2} are output resistance of M_1, M_2, respectively.

Although other high-gain topologies such as cascode can be used in the second stage, their significantly higher output impedance, severely limits the overall BW of the amplifier. Reducing the output impedance to meet the required BW while maintaining the gain, results in significantly higher power consumption in this stage. On the other hand, an inverter benefits from large equivalent transconductance that is effectively equivalent to the summation of those of the NMOS and PMOS transistors. This larger transconductance allows for higher gain with the same output impedance; therefore, larger BW can be achieved.

The presence of large capacitance at input node increases the noise of the TIA at higher frequency. Neglecting the noise contribution from 2nd stage and assuming that the dominant pole from the RGC stage is at the input, a valid assumption for much larger input capacitance in comparison with inter-stage parasitic capacitance, the input-referred noise of the TIA is:

$$\overline{i_{n,in}^2} \approx 4kT\left[\frac{1}{R_1}+\frac{1}{R_2\|R_{tune}}\right]+\frac{4kT\gamma\left(g_{d0,2}+g_{d0,3}\right)}{g_{m2}}.\left(\frac{1}{R_1^2}+\omega^2.C_{in}^2\right), \qquad (3.17)$$

where C_{in}, is the total capacitance at input terminal of the TIA, g_{d0} is the drain-source conductance at zero V_{DS}, and γ is the noise coefficient (~2/3 in long channel regime). Neglecting the noise contribution from the 2nd stage ensures that the input-referred noise does not see the effect of output pole that is due to the large parasitic capacitance of micromechanical resonator. For non-inverting operation where the output is directly taken out from RGC stage, the effect of output pole should be considered too.

The sustaining circuitry was fabricated in a 2P3M 0.5μm CMOS process. The IC included four TIAs; two RGC TIAs and two inverter TIAs that will be explained in the next section. Each two-stage TIAs has been accompanied by a similar TIA with same design parameters but without the switching network. Switching network is used for dual-mode operation. The switchless TIAs are used to determine the effect of switching network on the phase-noise performance of the oscillator. The die area is 1.4mm × 1.4mm (Fig. 3.22). Gain and frequency response measurement of the TIAs are performed by an Agilent E5071C Vector Network Analyzer (VNA) and are followed by oscillation spectrum and phase-noise measurement taken when the IC is wirebonded to micromechanical resonators. Agilent E4407 spectrum analyzer and E5500 phase-noise

measurement systems are used to monitor the oscillation spectrum and measure the phase-noise. An off-chip 50Ω buffer is used to drive the 50Ω input of the measurement equipment.

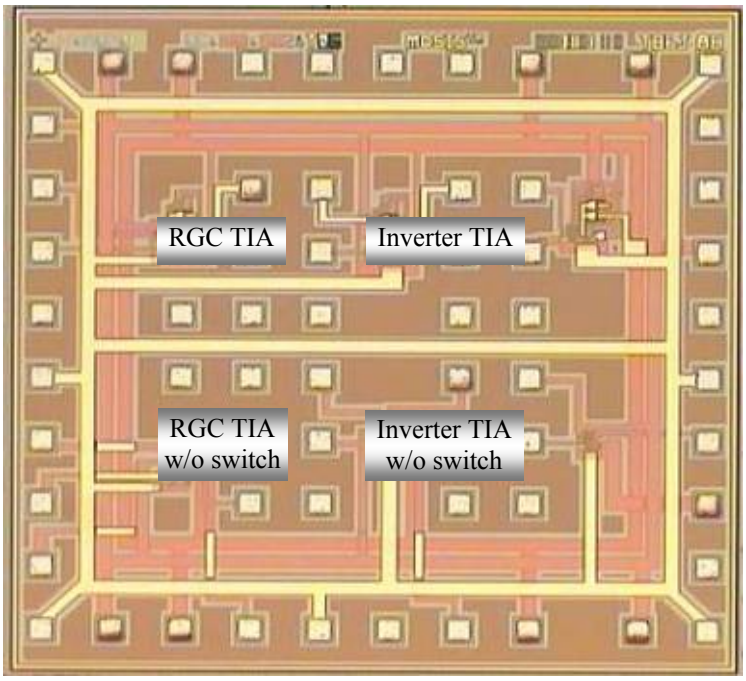


Fig. 3.22. Micrograph of the fabricated IC

The frequency response of the TIA for both modes of operation is measured individually. The parasitic shunt capacitance of the resonator is represented by shunt capacitance to ground, C_p, at both input and output terminals of the TIA. Since creating a precise AC current source is difficult, a novel method is used to determine the transimpedance gain and BW of the TIA. The signal from VNA is first passed through a series RC network and then given to the input of the TIA. The capacitor is used to DC-decouple the input of the TIA and the VNA (Fig. 3.23) and is chosen large enough for the frequency of interest. The transimpedance gain of the TIA, Z_{TIA}, can be found as:

$$Z_{TIA} = \frac{v_{out}}{i_{in}} = \frac{v_{out}}{v_s}.\left(R_s + Z_{in}\right), \tag{3.18}$$

where v_s is the source voltage from the vector network analyzer (VNA), v_{out} is the output voltage of the TIA and Z_{in} is the input impedance of the TIA. As evident from (3.18), choosing $R_s >> |Z_{in}|$, the low-frequency transimpedance gain is simply found:

$$Z_0 = \left|Z_{TIA}\right|_{w->0} = \frac{v_{out}}{i_{in}} \approx \frac{v_{out}}{v_s}.R_s \,, \tag{3.19}$$

where v_{out}/v_s is the voltage gain measured by the VNA. To measure the frequency response (esp. the BW) of the amplifier, R_s is reduced to the original 50Ω input impedance of the VNA source. Using the low-frequency gain of the TIA found in (3.19) and assuming that the input impedance of the TIA can be approximated as a parallel $R_{in}C_{in}$ tank, the location of poles and zeros can be found as:

$$\begin{aligned} Z_1 = \left|Z_{TIA}\right|_{\omega\to 0} &= \left|\frac{v_{out}}{v_s}.\left(50 + \frac{R_{in}}{R_{in}.C_{in}.s+1}\right)\right|_{\omega\to 0} \approx \left|\frac{v_{out}}{v_s}.(50+R_{in})\right| \,, \\ \Rightarrow \omega_z &\approx \frac{1}{(R_{in} \,||\, 50)C_{in}}, \omega_p = \frac{1}{R_{in}C_{in}} \end{aligned} \tag{3.20}$$

It is clear from (3.20) that $\omega_z < \omega_p$, therefore the BW of the measured response from the VNA is reasonably close to the 3-dB BW of the TIA. In this work, the maximum designed BW of the amplifier with 2pF capacitive load is less than 300MHz with dominant pole at input, therefore $R_{in} >> 50\Omega$.

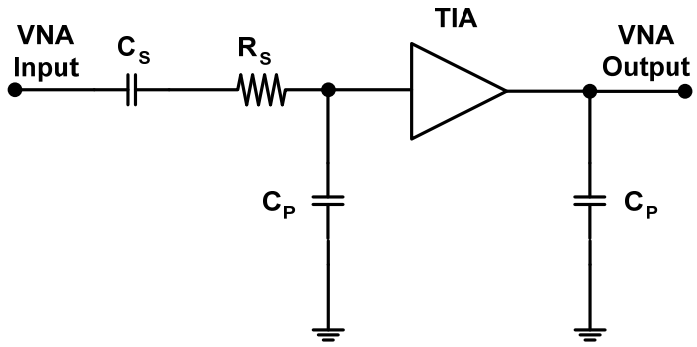


Fig. 3.23. Simplified schematic of the measurement setup

Using this method, the frequency response of the tunable two-stage RGC TIA is measured. When operating in non-inverting mode (the second stage is turned off), the TIA consumes 0.84mA from 3V supply and maintains transimpedance gain of 72dBΩ up to 40MHz (Fig. 3.24).

In inverting mode when both stages are on, the power consumption is increased by an additional 3.8mW. In this case, the BW of the TIA is extended beyond 170MHz with gain more than 66dBΩ. The gain tuning in second stage of the TIA allows for 10dB increase in the gain (without experiencing overshoot) at the expense of smaller BW~89MHz (Fig. 3.24).

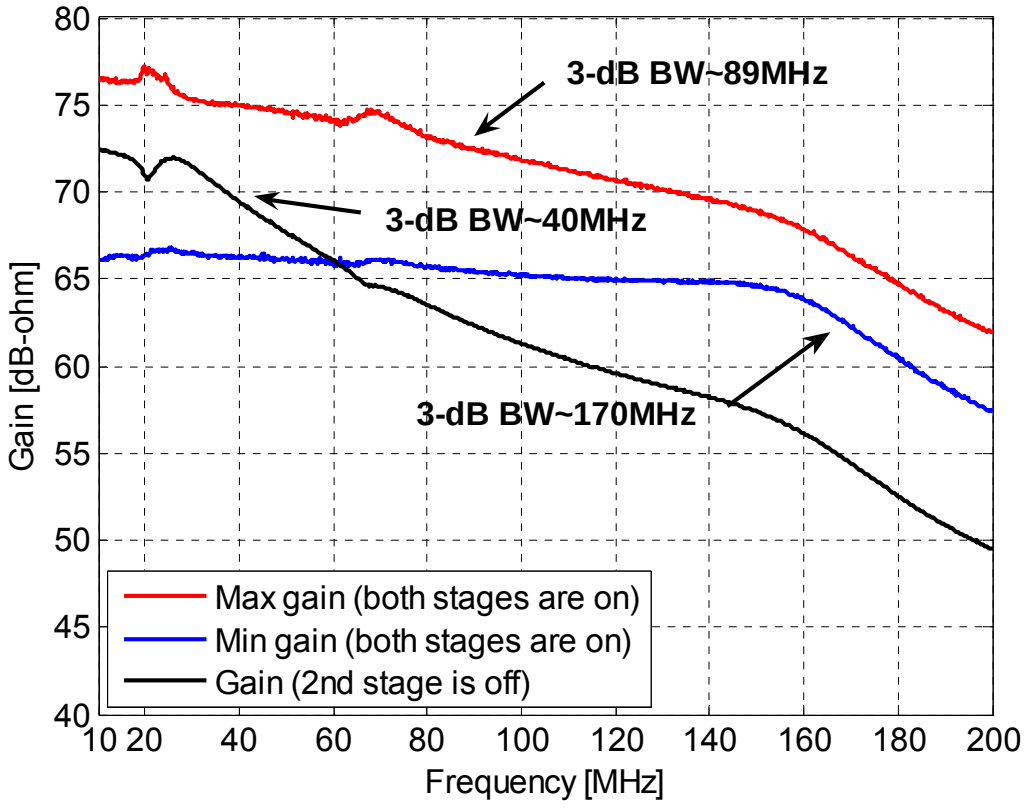


Fig. 3.24. Measured frequency response of the RGC TIA

The RGC TIA is interfaced with a 35MHz TPOS resonator (Q~10,100) and output spectrum is monitored with the spectrum analyzer. The oscillation is sustained when the supply voltage is increased to 2.14V and DC current is increased to 400µA. The oscillation starts at lower supply voltage of 1.9V in vacuum and the power consumption is reduced to 580µW (Fig. 3.25). This is mainly due to the lower loss of the resonator when operating under vacuum. The phase-noise of the oscillator in air and under vacuum is measured at V_{DD}=2.5V (P_{DC}=1.6mW) and are compared with each other (Fig. 3.25). The measured phase-noise of the oscillator at 1kHz offset is -103dBc/Hz in air and -111dBc/Hz under vacuum. The phase-noise floor, which is dominated by the TIA and off-chip buffer noise, reaches -140dBc/Hz. Close-to-carrier phase-noise performance between offset frequencies of 10Hz and 1kHz, is improved by ~ 10dB.

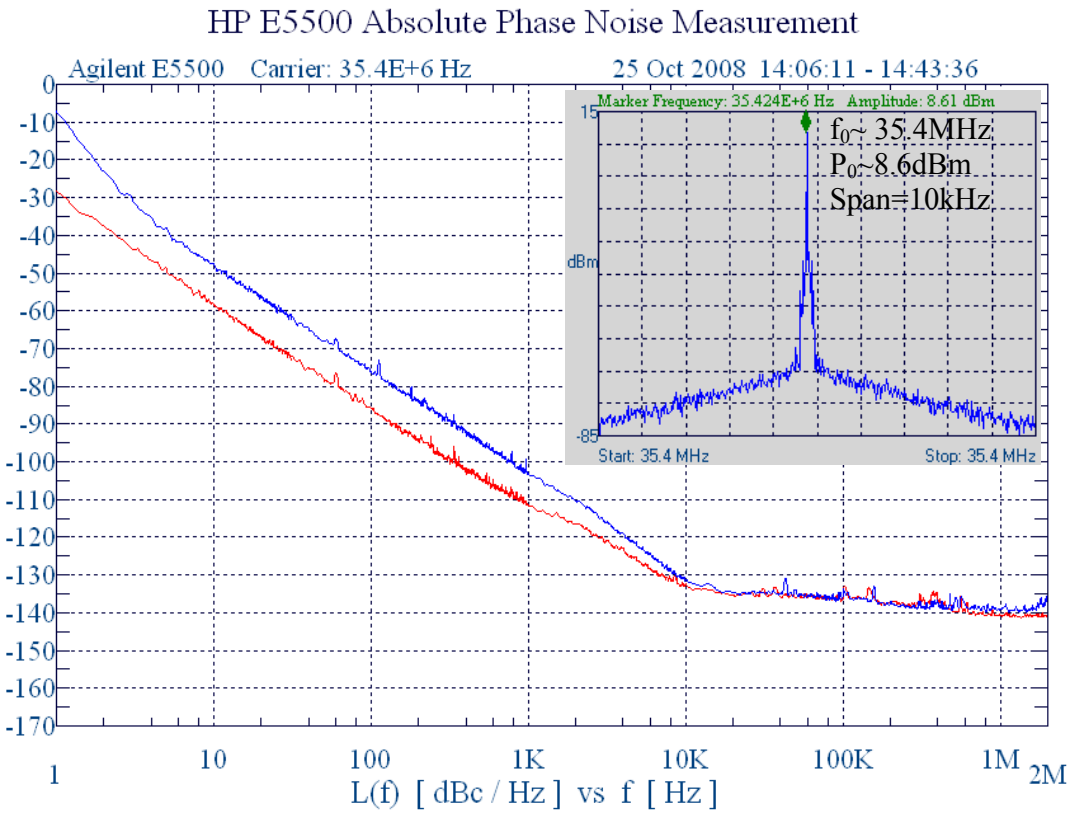


Fig. 3.25. Spectrum and phase-noise of the 35MHz oscillator made with RGC TIA

3.6.2 Inverter TIA

An inverter TIA is designed and included on the same chip that the RGC TIA is fabricated on. The TIA benefits from two high-gain stages; an inverter with tunable shunt-shunt feedback resistor that acts as the current-to-voltage conversion stage is followed by a CS voltage amplifier with resistive load (Fig. 3.26). This TIA is designed for larger GBW and naturally, consumes more power. When operating in non-inverting mode, both inverting stages are in the loop to ensure in-phase operation; in inverting mode, the second stage is bypassed, leaving an inverter with adjustable gain and 180º phase-shift.

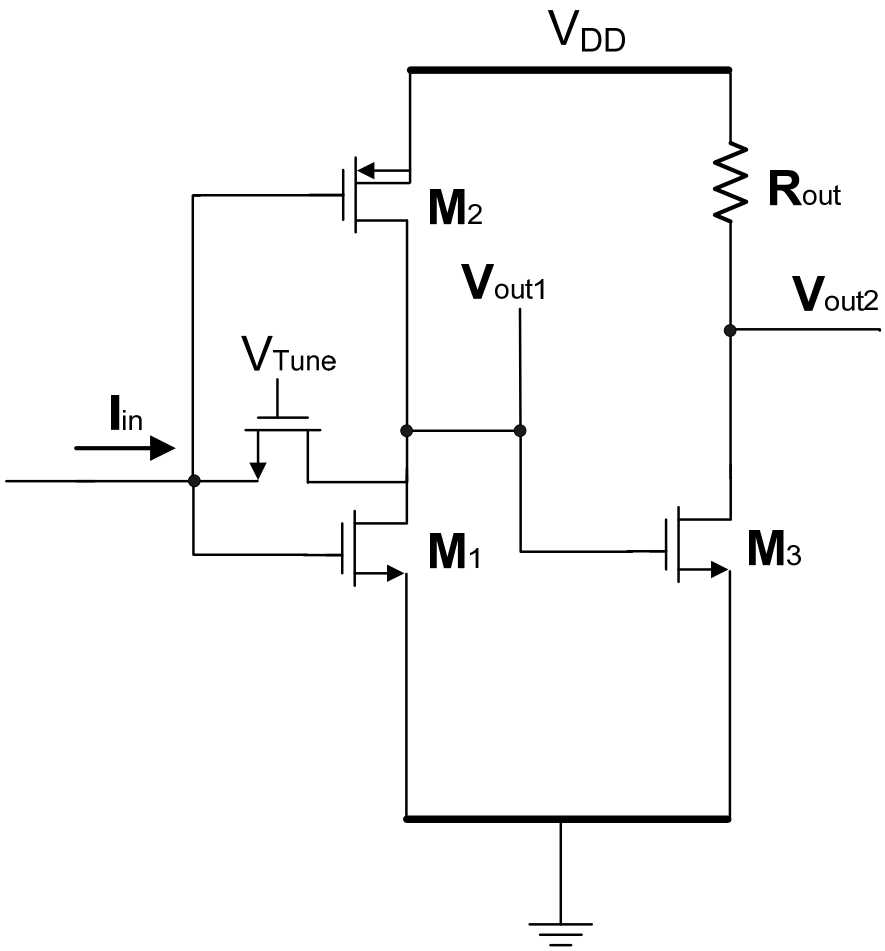


Fig. 3.26. Schematic of the Inverter TIA

For high-frequency operation, both input and output resistances of the sustaining amplifier have to be minimized. In addition, all inter-stage nodes have to be provided with a low- impedance path to ground to avoid a low frequency pole.

Due to the high gain of the inverter, the transimpedance gain is mainly determined by the tunable shunt-shunt resistor, R_{tune}. The equivalent input resistance of the closed-loop system is:

$$R_{in} \approx \frac{R_{tune} + \left(r_{o1} \| r_{o2}\right)}{\left(g_{m1} + g_{m2}\right)\left(r_{o1} \| r_{o2}\right)}, \tag{3.21}$$

where g_{m1} and g_{m2} are transconductance, and r_{o1} and r_{o2} aredrain source resistance of M_1 and M_2 transistors, respectively. The second stage of the TIA is a CS with resistive load. Careful trade-off of gain with BW obviates the need for additional high-power output stage. The transimpedance gain of the TIA is:

$$R_{CL,Inverter} \approx -R_{tune}.A_{v2} \approx g_{m3}.R_{tune}.R_{out}, \tag{3.22}$$

where A_{V2} is gain of the 2nd stage and g_{m3} is the transconductance of M_3. Neglecting the noise contribution from 2nd stage and assuming that the dominant pole is at the input, the input-referred noise of the TIA is:

$$\overline{i_{n,in}^2} = 4kT.\omega^2.C_{in}^2.\left[\frac{\gamma\left(g_{d0,1} + g_{d0,2}\right)}{2R_{tune}^2.\left(g_{m1} + g_{m2}\right)^2} + \frac{1}{R_{tune}}\right], \tag{3.23}$$

Using the method specified in section A, the frequency response of the tunable two-stage Inverter TIA is measured. When operating in inverting mode (2nd stage off) the TIA consumes 1.6mA from 3V supply and provides more 74dBΩ up to 72MHz. The BW can be extended beyond 127MHz at the expense of 13dB lower gain (Fig. 3.27).

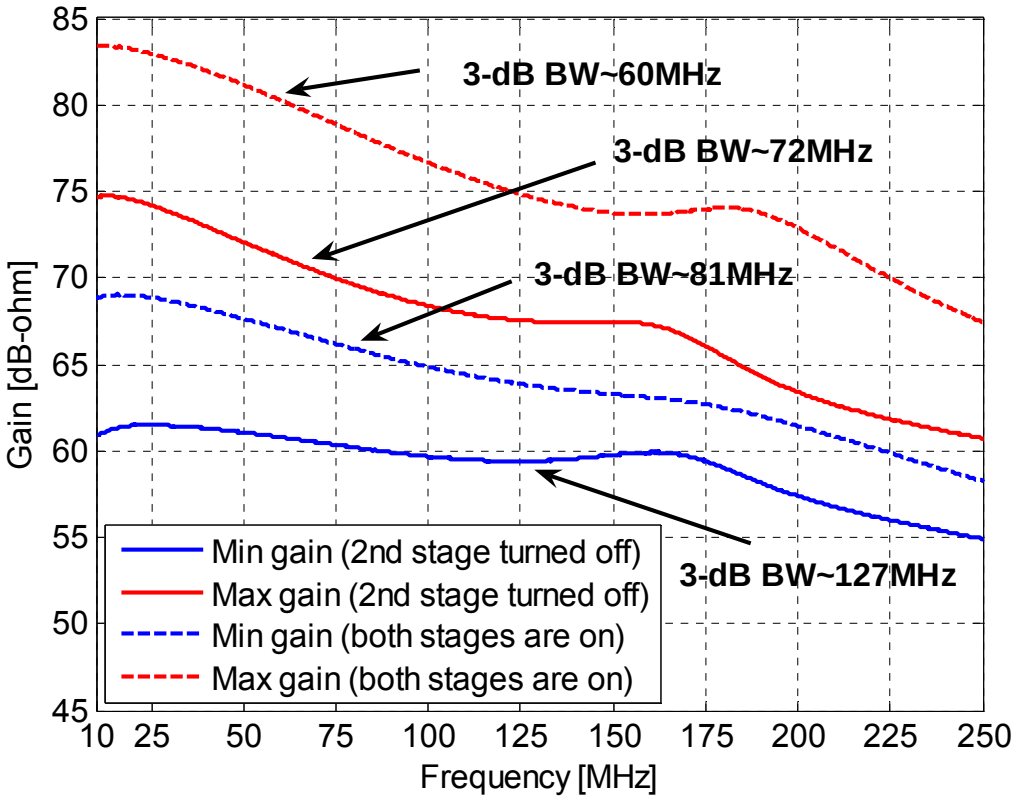


Fig. 3.27. Measured frequency response of the Inverter TIA (V_{DD}=3V)

In non-inverting mode (both stages on), the power consumption is increased by 3.4mW. The BW of the TIA is ~ 60MHz with gain more than 83dBΩ. The gain tuning in the first stage allows for 21MHz improvement in BW at the expense of smaller gain~68dBΩ (Fig. 3.26). Increasing the supply to 5V enables BW > 220MHz (Fig. 3.28).

The Inverter TIA is interfaced with the same 35MHz TPOS resonator that is used in previous section, and the output spectrum is monitored with a spectrum analyzer. The oscillation is sustained when the supply voltage is increased to 1.75V and DC current is increased to 280μA. The oscillation starts at lower supply voltage of 1.62V under

vacuum and the power consumption is reduced to 260μW (Fig. 3.29). This is mainly due to the lower loss of the resonator under vacuum.

The phase-noise of the oscillator in air and under vacuum is measured at V_{DD}=2.5V (P_{DC}=3.8mW) and are compared with each other (Fig. 3.29). The measured phase-noise of the oscillator at 1kHz offset is -105dBc/Hz in air and below -114dBc/Hz under vacuum. The phase-noise floor, which is dominated by the TIA and off-chip buffer noise, reaches -142dBc/Hz. When comparing the phase-noise performance of this oscillator with the one that is made with the RGC TIA, substantial improvement in the close-to-carrier performance is clearly visible.

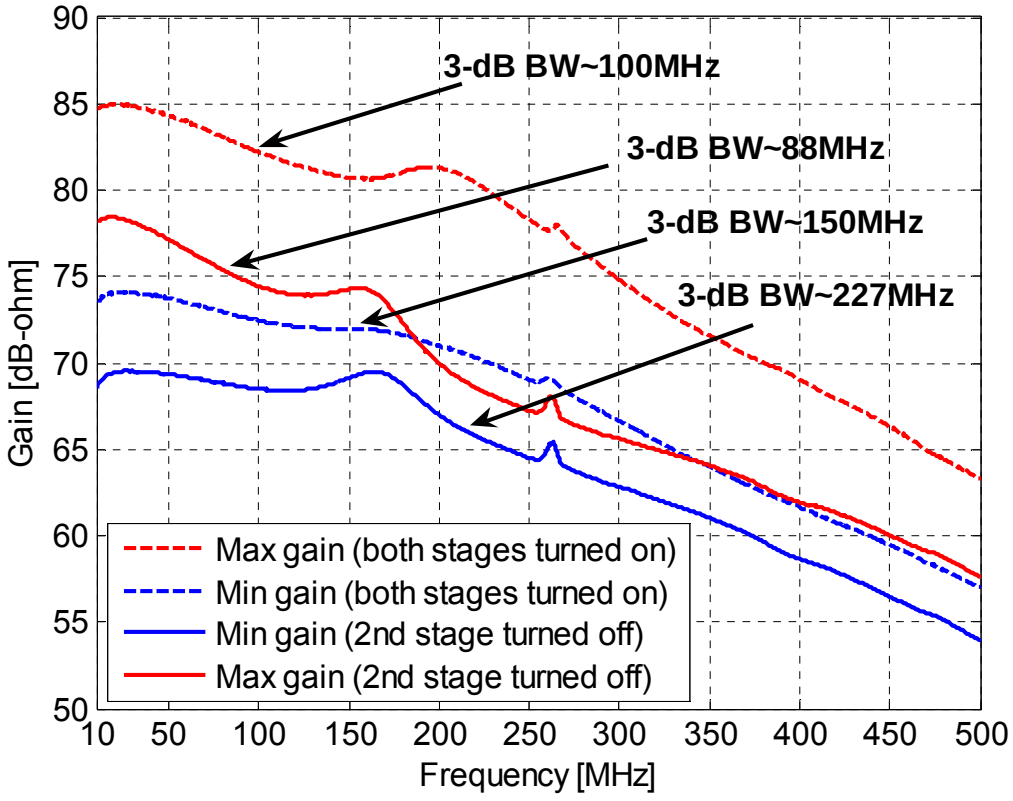


Fig. 3.28. Measured frequency response of the Inverter TIA (V_{DD}=5V)

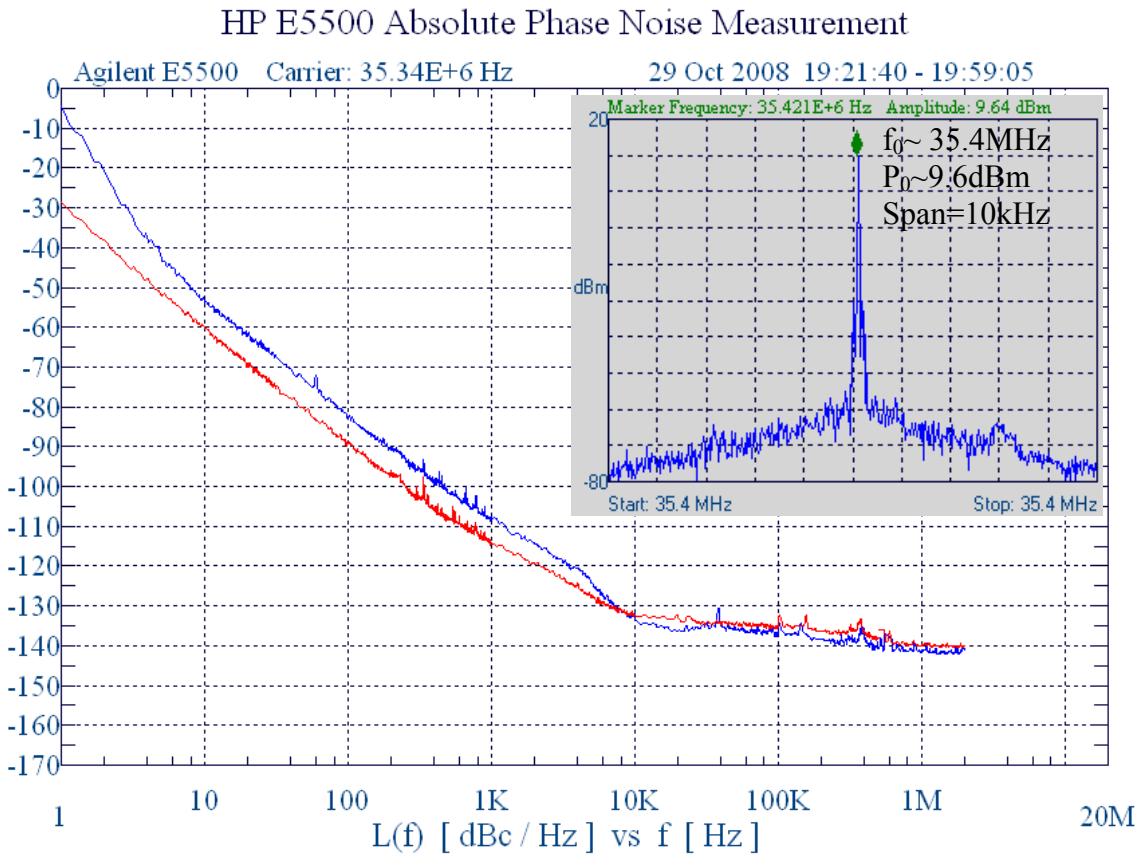


Fig. 3.29. Spectrum and phase-noise of the 35MHz oscillator made w/ Inverter TIA

3.6.3 Multiple-Stage Feedback TIA

To realize an oscillator in the UHF range using a lossy micromechanical resonator with large input/output parasitic capacitance (~2pF), it is crucial to use high-gain broadband TIA. To this end, a three-stage feedback TIA with variable gain at the first stage is designed (Fig. 3.30) [7]. The TIA was intended to be a universal design, capable of sustaining oscillation with a broad range of resonators having characteristics of: 100MHz $< f <$ 1GHz and 50Ω $< R_m <$ 1kΩ.

To achieve high gain while maintaining the wideband characteristic of the TIA, a low-gain transimpedance stage is followed by two wideband voltage gain stages. Shunt-shunt

feedback is introduced in each voltage gain stage to reduce the impedance at the inter-stage nodes. This technique increases the frequencies of the poles resulting from the inter-stage nodes to much higher than those of the input/output; thus providing wideband characteristic without increasing the power consumption. Another advantage of this technique is to eliminate on-chip inductors typically used in high-gain gigabit CMOS TIA circuits to enhance the bandwidth. The result is significant reduction in area.

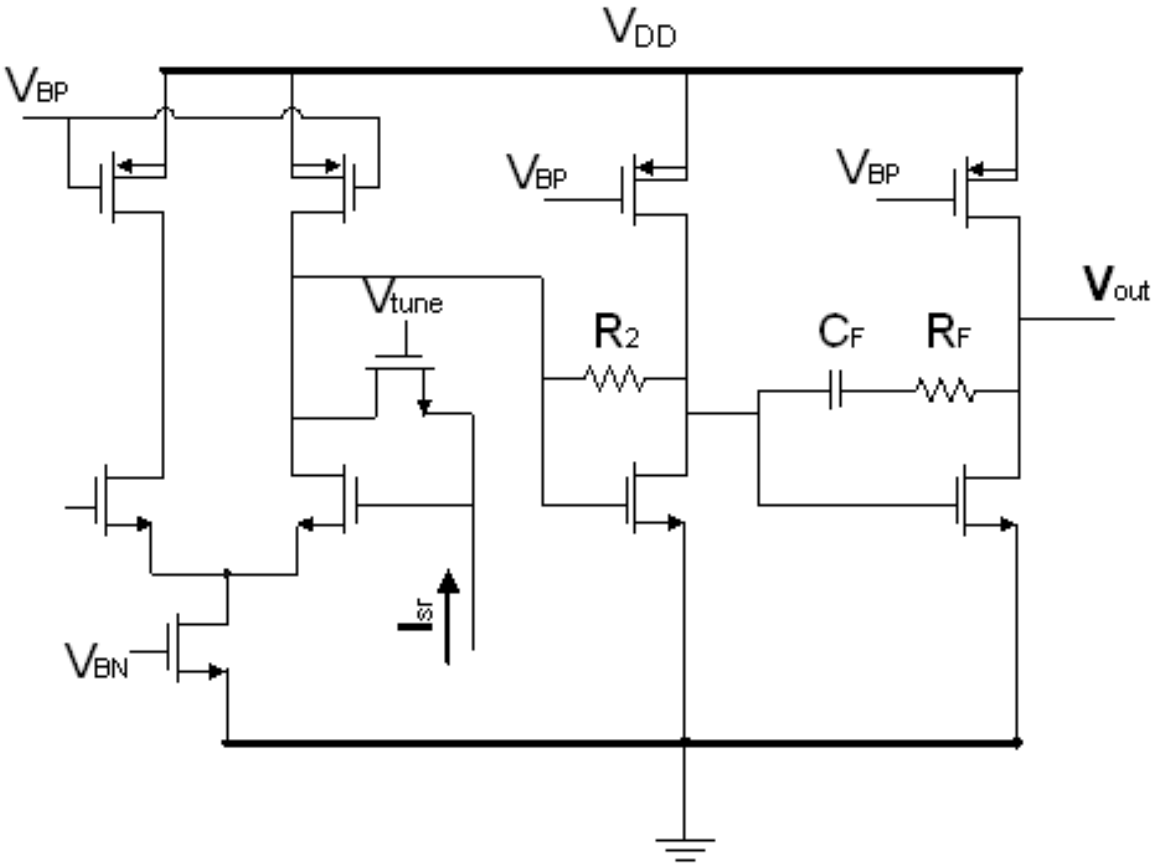


Fig. 3.30. Schematic of the three-stage tunable feedback TIA (biasing not shown)

The designed TIA achieves BW > 880MHz at maximum gain (72dBΩ) when loaded with 2pF capacitance load at the input and output node. The main reason to choose common source over higher gain topologies such as cascode is to increase the voltage swing and enable the circuit to operate from lower supply (in this case 1.5V) that further reduces the

power consumption. The higher output swing results in lower phase-noise floor as the dynamic range of the TIA will be improved.

To boost the gain at higher frequencies, capacitive coupling is used in the third stage. The high pass response of the third stage significantly attenuates the low frequency noise of the amplifier, which is higher in CMOS circuits due to large flicker noise. Therefore, the contribution of TIA noise to the overall close-to-carrier phase-noise is reduced. The choice of capacitor C_F determines the attenuation. For the case of 2pF, the phase-noise at 1kHz offset is 2dB lower than the oscillator constructed with the same resonator but using the TIA without capacitive coupling.

The TIA and biasing circuitry is fabricated in a 0.18um 1P6M CMOS process. Another TIA that does not incorporate capacitive coupling was also fabricated on the same die for the purpose of performance comparison. An off-chip 50Ω buffer is used to interface with the measurement equipments. The TIA was measured to have maximum transimpedance gain of more than 71.8dBΩ and maximum BW in excess of 960MHz when loaded with 2pF at both input and output nodes. The TIA BW when interfaced with standard photodiodes with equivalent capacitance ~500fF will be enhanced to 1.5GHz. The TIA gain could be varied by 8dB (Fig. 3.31). The amplifier and biasing circuitry consumed 6.2mA from 1.5V supply. The die size is $1mm^2$ of which 450μm × 330μm is occupied by the sustaining amplifier (Fig. 3.32).

This three-stage feedback TIA is interfaced with a 496MHz AlN-on-Si ($Q_{unloaded}$~3,800) TPOS resonator. The output power of the 496MHz oscillator is ~2dBm. The measured phase-noise of the oscillator in air is –92dBc/Hz at 1kHz offset and below –147dBc/Hz at far-from-carrier (Fig. 3.33). The measurement was carried out by an Agilent EE5500 phase-noise analyzer. The oscillation power was 1.9dBm, well within the resonator linear range. The slight degradation in phase-noise performance around 100kHz offset is due to the internal phase-noise limit (~–136dBc/Hz) of the Agilent E8257C Analog Signal Generator that is used in the phase-noise measurement setup. The spurs below 1kHz are caused by 60Hz signal and its harmonics.

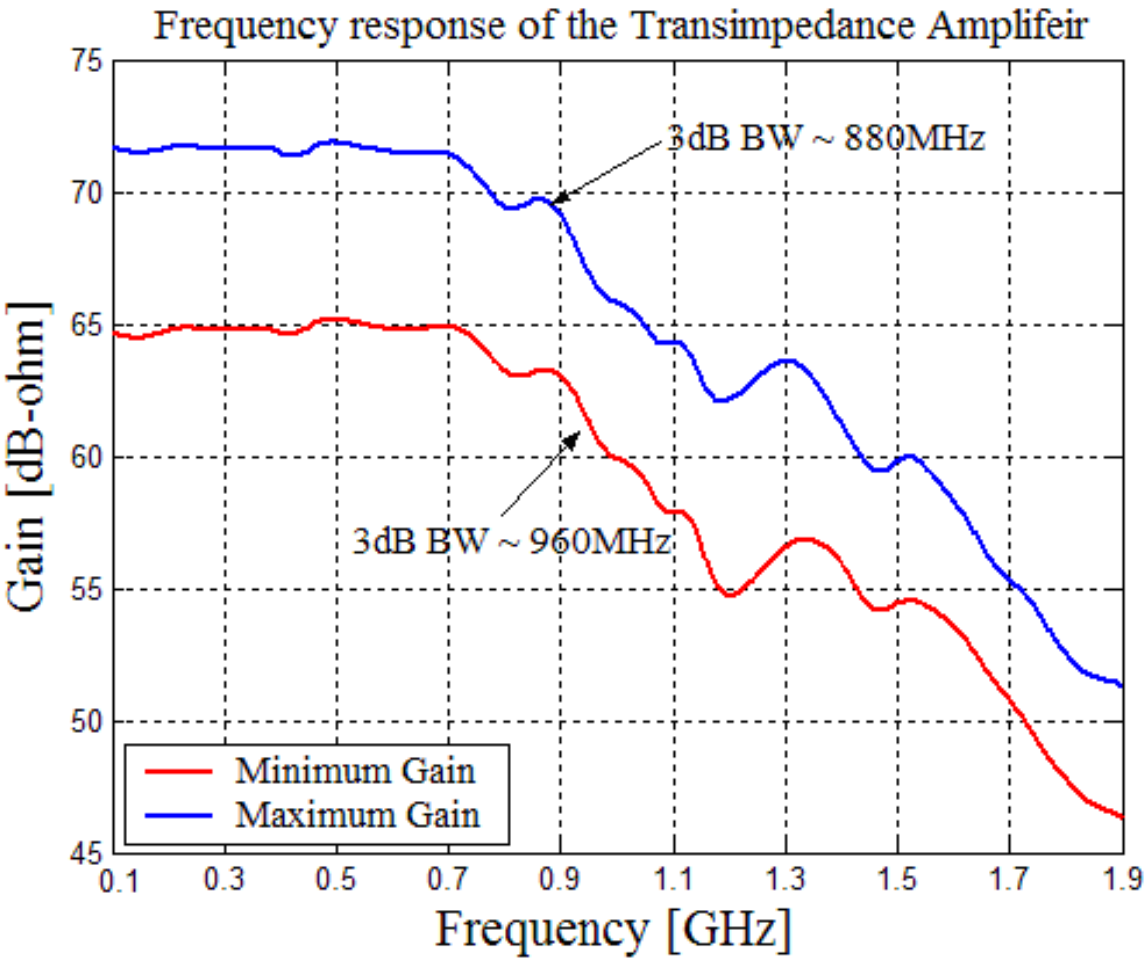


Fig. 3.31. Measured gain of the three-stage feedback TIA

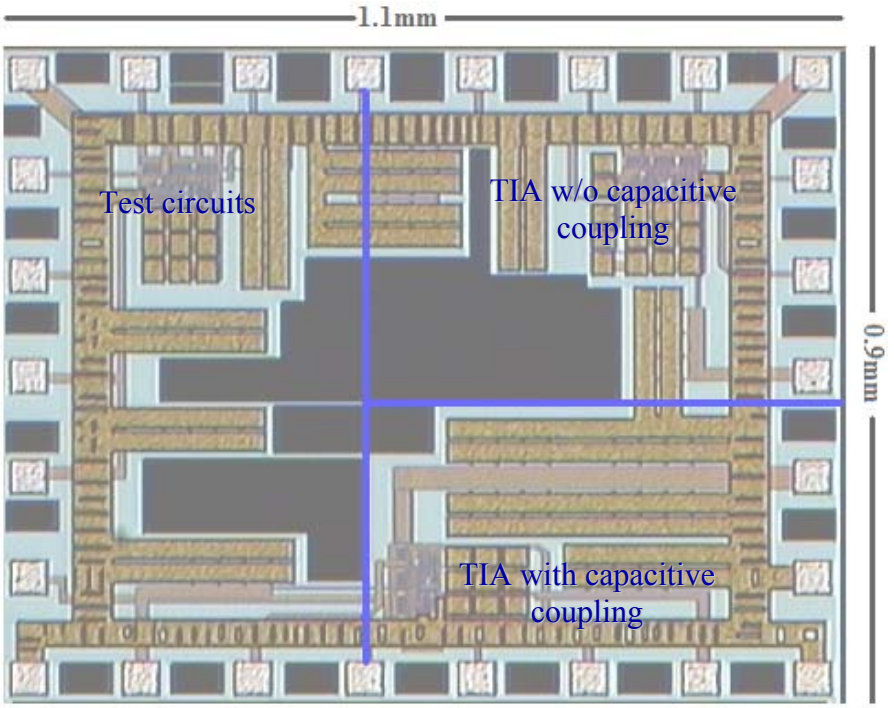


Fig. 3.32. Micrograph of the fabricated die

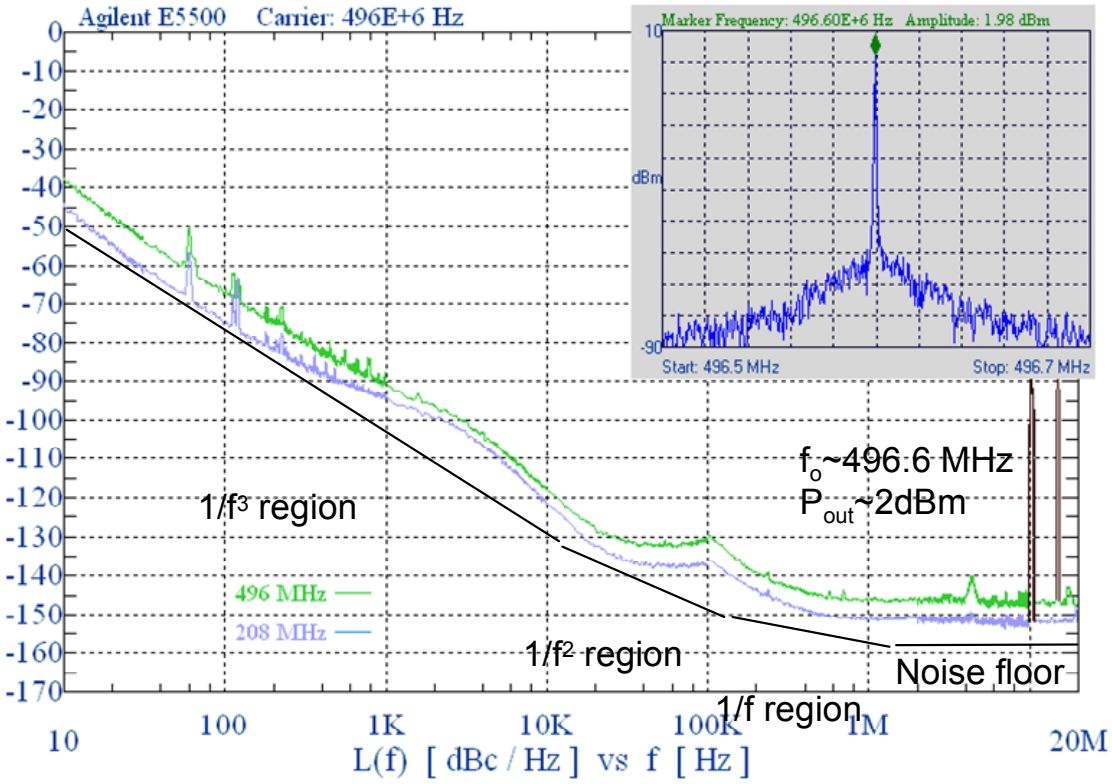


Fig. 3.33. Phase-noise of the 208MHz and 496MHz oscillators

3.6.3 TIA with Inductive Shunt Peaking

The BW enhancement techniques that were introduced so far take a high toll either on the power consumption or the noise performance of the TIA. The open-loop architectures are known for higher input-referred noise. The feedback approach forces trade-off of gain and BW, leaving no choice but to increase the power consumption when both high gain and BW are desired. A logical conclusion would be to combine feedback approach and pole cancellation to simultaneously increase the BW while meeting the required transimpedance gain specification. In this section, a two-stage high-gain broadband differential CMOS TIA that uses inductive shunt peaking is presented (Fig. 3.34).

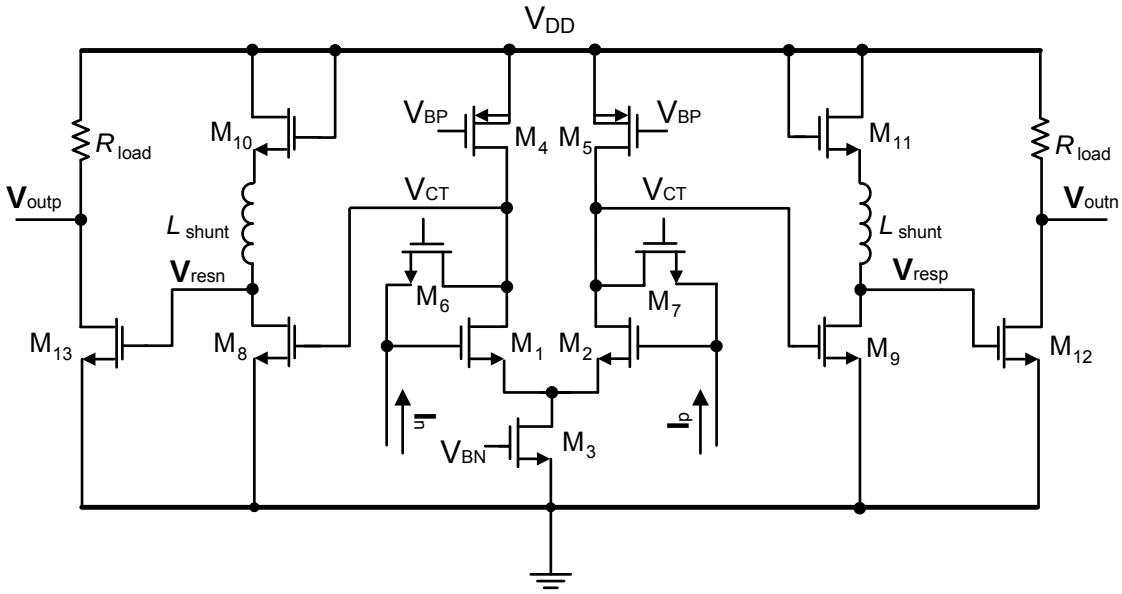


Fig. 3.34. Schematic of the two-stage differential TIA with inductive shunt peaking

The TIA uses feedback in the first stage to provide large BW and good noise matching when used in micromechanical oscillator applications. The gain tuning is incorporated in this stage by varying the equivalent resistance of the MOS resistor. The gain is further increased b cascading an additional CS stage to the first stage. The 2nd stage uses inductive shunt peaking to cancel the effect of output pole that is resulted from large shunt parasitic capacitance of the micromechanical resonator. A diode-connected NMOS

transistor is placed in series with the inductor to increase the resistive load of this stage and increase the gain. The value of this resistance is carefully chosen to meet the required gain specification for the overall TIA. Finally, a 50Ω-matched CS output buffer stage is added to interface the output of the TIA with the 50Ω input impedance of measurement equipments. The advantage of differential signaling is the common-mode rejection that helps suppress the noise injected from supply and other bias circuits. Moreover, it helps improve the stability by minimizing the effect of parasitic inductances that appear at critical nodes such as the reference ground. The two-port nature of most high-frequency lateral micromechanical resonators makes the fully-differential operation challenging. Therefore, the common-mode feedback (CMFB) circuitry is not included in this pseudo-differential TIA.

The TIA is designed and fabricated in 0.13μm process. Due to the lack of proper equipment for fully-differential gain and noise measurement, only the simulated data is presented here. The TIA is capable of providing ~64dBΩ (Fig. 3.35) and BW>1.7GHz with 2pF input/output capacitive load while consuming 9.8mW (including the on-chip buffer). The differential gain can be tuned up to 72dBΩ at the expense of reduction in BW (~1.2GHz). The TIA noise is simulated with 2pF input and output capacitive load. Due to pole cancellation at the output, the dominant pole is at the input of the TIA. The simulated input-referred current noise is 5.3pA/√Hz @1GHz (Fig. 3.36). Although this data could be very valuable to understand the noise mechanism and help with optimization process, it is of little practical value due to the absence of proper gate-induced noise model in the BSIM3.1 transistor models that are used in this work.

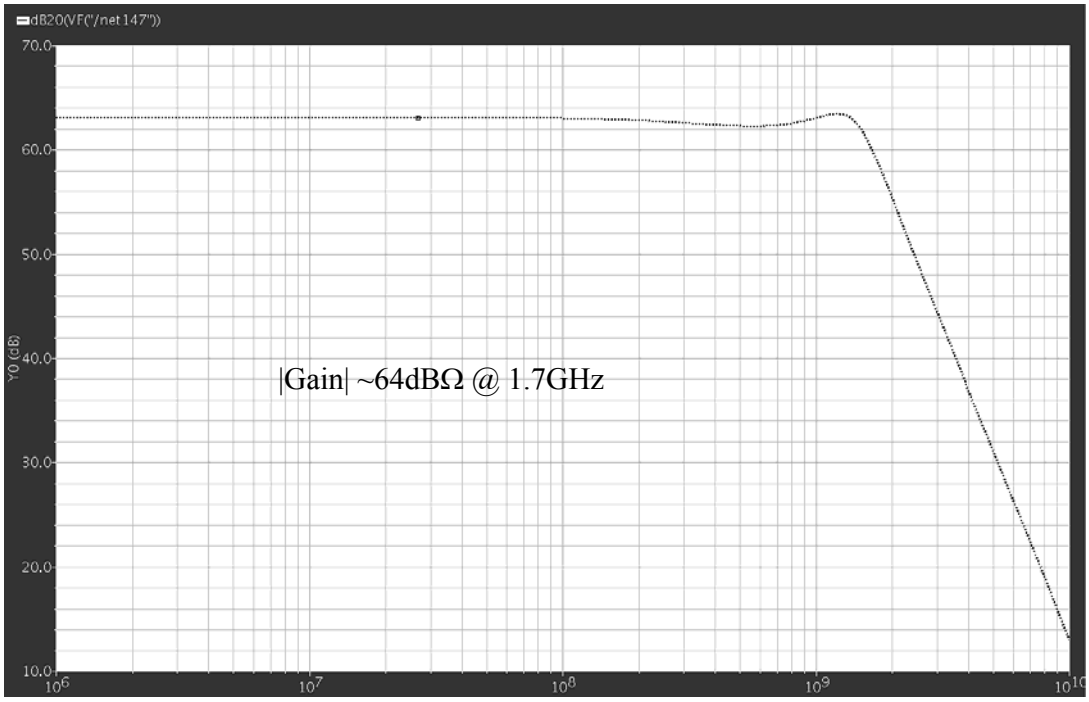


Fig. 3.35. Differential transimpedance gain of the TIA with inductive shunt peaking

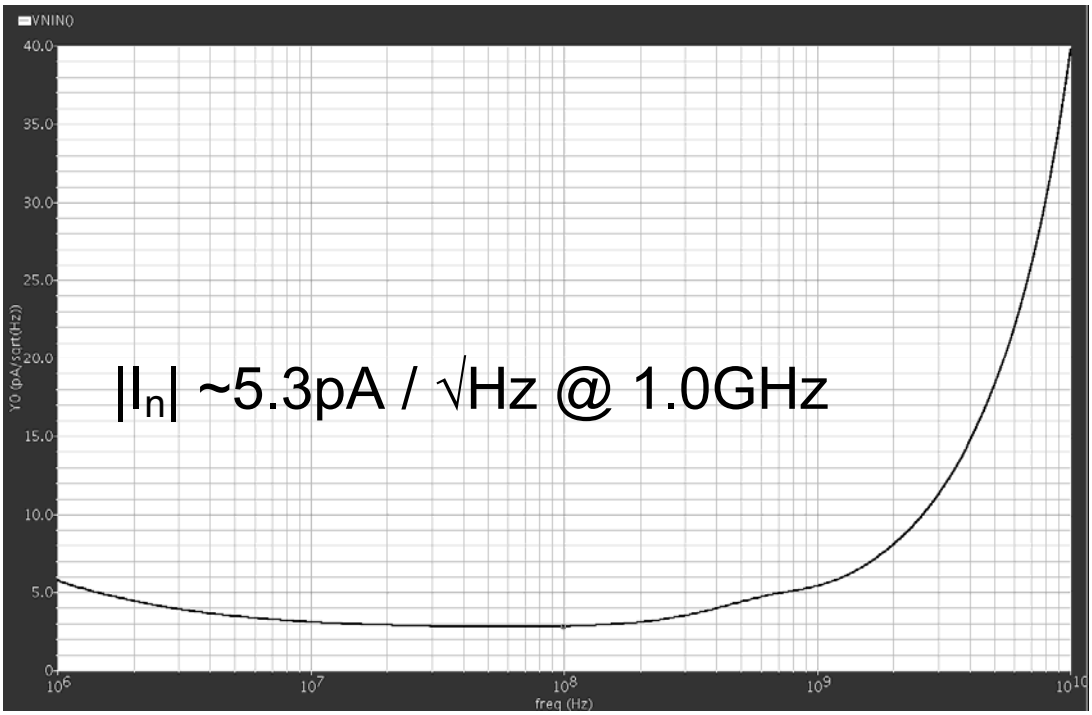


Fig. 3.36. Input-referred current noise of the TIA

To benchmark the TIA performance for micromechanical oscillator applications, the TIA is interfaced with a 206MHz AlN-on-Si resonator with relatively low-Q (~1,200) and high motional impedance (~600Ω). The oscillator achieves phase-noise better than -78dBc/Hz at 1kHz offset but the far-from-carrier performance is not impressive (Fig. 3.37). This is due to the limited dynamic range of the 2nd stage that uses a diode-connected NMOS in the load. This poor phase-noise performance combined with large inductors used for shunt peaking (7.5nH each), makes the TIA unattractive for low phase-noise micromechanical oscillators.

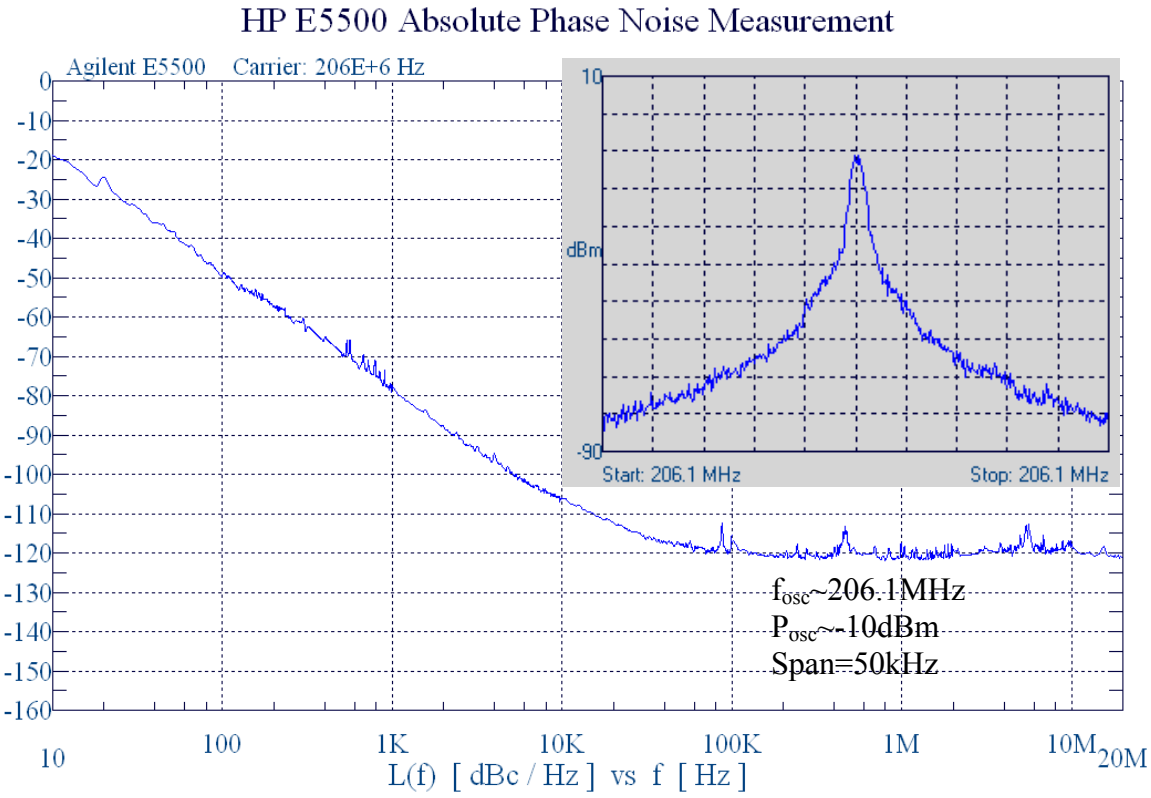


Fig. 3.37. Spectrum and phase-noise of the 206MHz AlN-on-Si oscillator

3.6.5 TIA with Current Pre-Amplifier

High Q lateral-mode silicon micromechanical resonators are suitable for multi-frequency references but exhibit high motional resistance compared to FBAR. The motional

resistance can be reduced at the expense of larger transduction area and hence larger parasitic capacitance. This high motional resistance combined with large parasitic capacitance of the resonator makes the realization of low-power oscillator complicated. As such, the development of low-power high-gain transimpedance amplifiers (TIA) becomes necessary.

The most popular TIA topology used in micromechanical oscillators is the shunt-shunt feedback TIA as it improves the BW and reduces the input-referred noise [6], [7]. The BW improvement forces a trade-off with the gain. Further increase in the gain requires higher power consumption that is undesirable. Using a broadband current amplifier increases the gain while maintaining the BW with little or no extra power consumption.

In this section, an inductor-less 0.18µm CMOS tunable TIA that uses a broadband current pre-amplifier for gain boosting is presented [66]. The measured gain is varied from 64dBΩ to 76dBΩ in a BW of 1.7GHz to 2.1GHz with 2pF input/output load. The TIA consumes 4.8mA from 1.5V supply.

Fig. 3.38 shows the TIA schematic and consists of 3 sections: current pre-amplifier that is combined with the current-to-voltage conversion stage, voltage amplifiers and 50Ω buffer. The first stage uses a broadband current amplifier to achieve gain with minimal effect on BW. The current gain is set by the W/L ratio of M_3 to M_1 transistor (N). The amplifier is a modification of inherently-low input resistance current-mirror ($\sim 1/g_{m1}$)

topology that is suitable for reducing the power consumption. The feedback further reduces the input resistance by a factor ~ $g_{m2}r_{ds2}$. Neglecting the effect of M_5:

$$R_{in} = \frac{1}{g_{m1}(1 + g_{m2}r_{ds2}) + g_{ds1} + g_{ds4}} \approx \frac{1}{g_{m1}g_{m2}r_{ds2}}, \tag{3.24}$$

where g_{m1}, g_{m2} are transconductances of M_1 and M_2, and g_{ds1}, g_{ds2}, g_{ds4} are drain-source conductance of M_1, M_2, and M_4, respectively. Current-to-voltage conversion is also performed in this stage; the current flowing through drain of $M_1$is mirrored into M_3 and passed through a resistive load to produce a voltage. Using small resistors ensures minimal effect on BW. The transimpedance gain in the first stage can be written as:

$$R_z \approx N\left(R_1 \,||\, r_{ds3}\right), \tag{3.25}$$

where N is the gain of the current mirror, R_1 is the load resistance, and r_{ds3} is the drain-source impedance of M_3. The power consumption of the first stage is ~3mW.

The voltage amplifier is a modified cherry-hooper that consists of two common source (CS) stages with gain tuning in second stage. Shunt-shunt feedback reduces the input and output impedance of the last stage, which in turn, help increase the BW by pushing the poles to higher frequency. Using a tunable PMOS resistor in the feedback network improves the linearity, lowers the noise contribution, and makes the TIA capable of interfacing with variety of micromechanical resonators with different loss. The resistive feedback is replaced with an RC network to create a zero whose frequency can be tuned to cancel the effect of the output pole.

To obtain the frequency response, two sets of S-parameters, one for maximum and the other for minimum gain were measured and interfaced in ADS with an ideal AC current

source with 2pF load. Gain > 76dBΩ with BW~1.7GHz is achieved. The gain can be tuned to 64dBΩ with BW > 2.1GHz (Fig. 3.39). Replacing the 2pF load with a photo-diode (C_p~500fF), the BW is extended to 2.5GHz with gain > 76dBΩ.

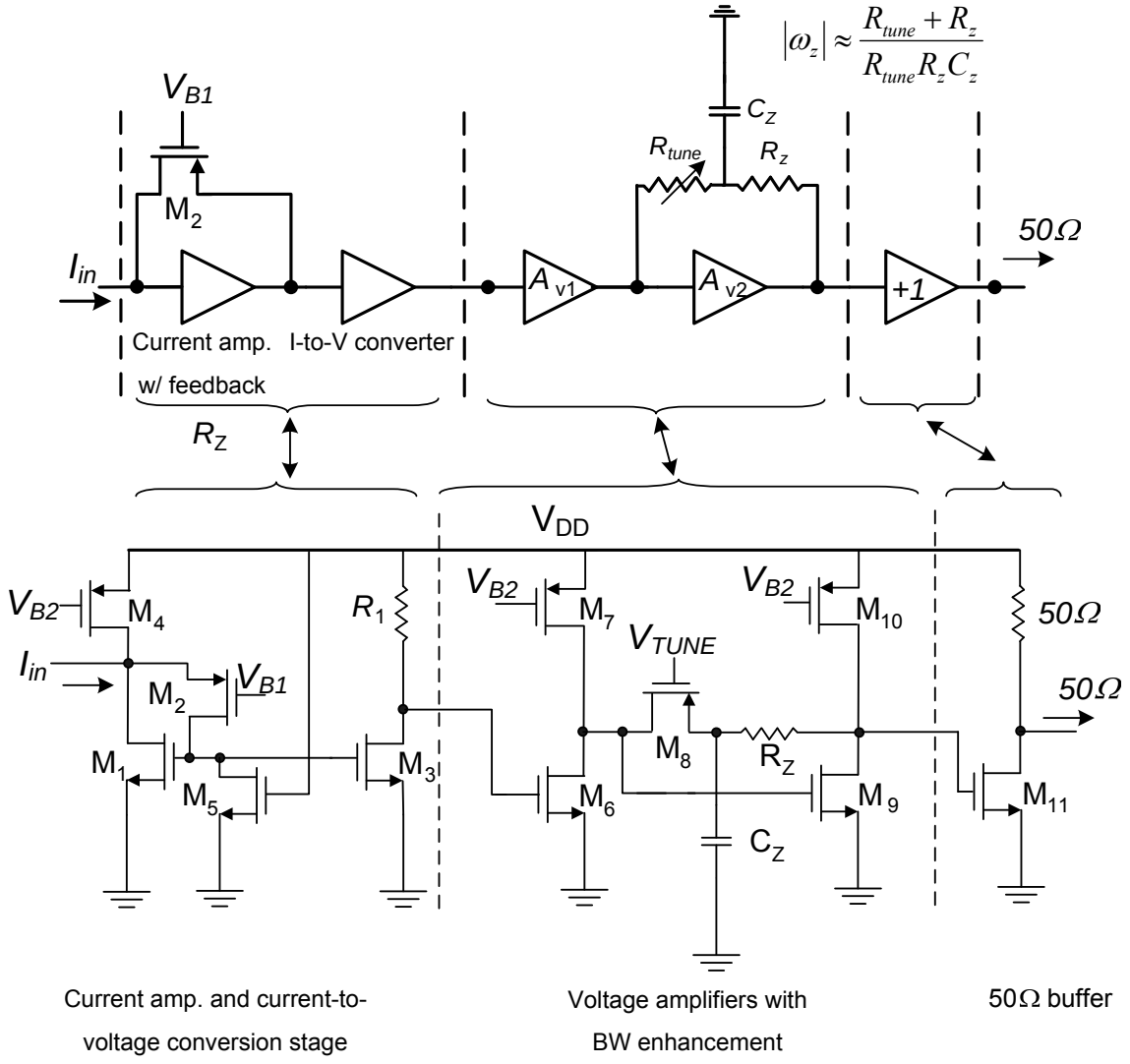


Fig. 3.38. Schematic of the TIA with current amplification stage

To measure the input-referred noise of the TIA, the input is connected to ground through a 2pF capacitor to emulate the loading of the resonator. The gain is set to maximum and the output signal is recorded from 10MHz to 5GHz. Due to the very small BW of the resonators, spot noise at a particular frequency is a more relevant performance metric

than the average noise (Fig. 3.40). Optimization of input transistor parameters has yielded an input-referred noise current of less than 7pA/√Hz in the 100-900MHz range.

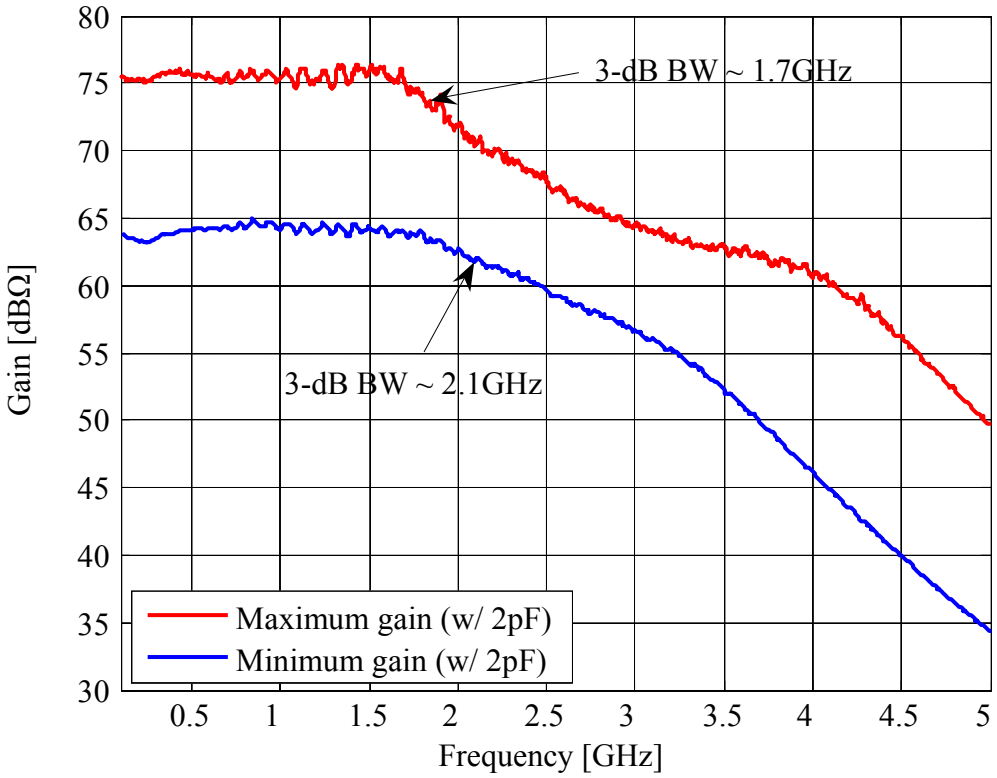


Fig. 3.39. TIA gain when the S-parameters are interfaced with ideal current source

Due to the large power handling of AlN-on-Si resonators [7], the oscillation power is set by nonlinearity of the TIA. As such, the dynamic range and gain compression of the TIA have direct impact on the performance of the oscillator. The use of relatively wide-swing CS output stage with feedback has pushed maximum output swing, which directly influences the overload current, beyond $0.62V_{p\text{-}p}$. Considering the input-referred noise of 7pA/√Hz in the 100-900MHz, the TIA achieves a remarkably high dynamic range of 138dB in this range. To obtain the 1-dB compression point (P_{1dB}), the S-parameters of the TIA in maximum gain setting is measured when the input power is varied from -20dBm

to -10dBm. The input-referred P_{1dB} (after 10dB adjustment due to the reflection) is -22dBm. The BW is only reduced by 8% to 1.6GHz (Fig. 3.41). The linearity is improved due to the use of low-gain output stage with tunable shunt-shunt feedback in the amplifier section. The TIA performance is compared with the state-of the-art 0.18 µm CMOS TIAs [67]-[70] (Table 3.1). When interfaced with a photo-diode (C_p~500fF), the TIA achieves a figure of merit of 2190 GHz.Ω/mW (GBW per DC power).

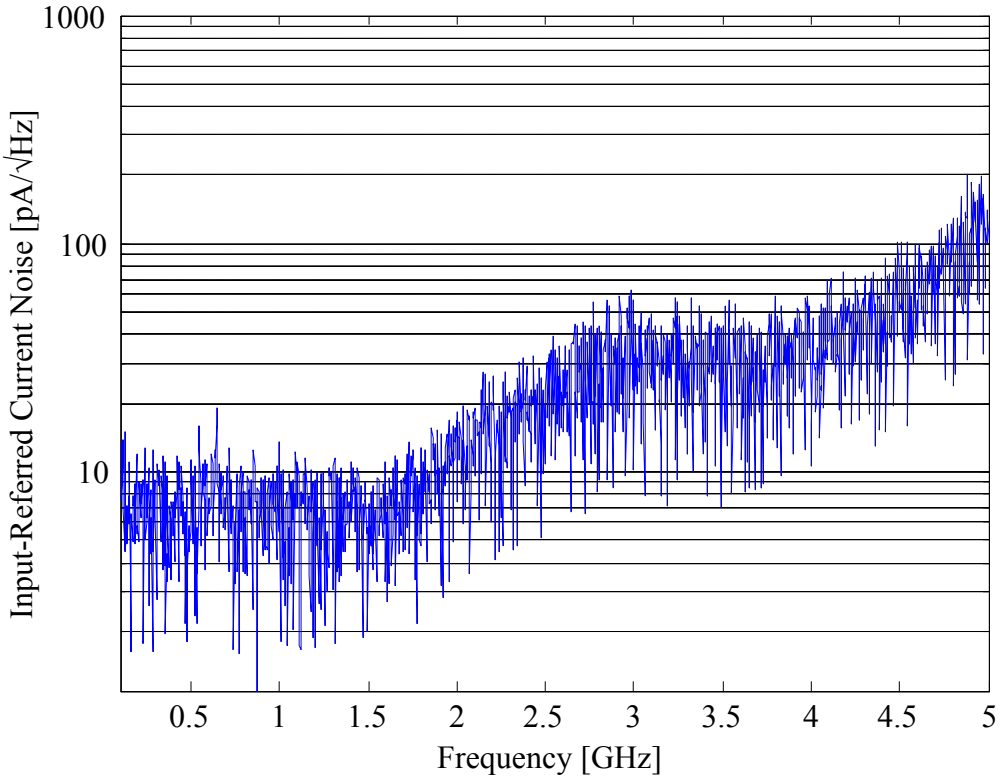


Fig. 3.40. Measured input-referred noise of the TIA with 2pF input load

To demonstrate its high performance, the TIA is interfaced with two high order lateral-mode micromechanical resonators: a high-loss 724MHz ($Q_{unloaded}$~2000, R_m ~ 750Ω, C_p~1.5pF) and a high-parasitic 1.006GHz ($Q_{unloaded}$~7100, R_m ~ 150Ω, C_p~3.2pF) AlN-on-Si resonators. The Q of 1.006GHz resonator is improved by optimizing the resonator

geometry and the anchors to minimize the acoustic loss by confining the energy in a single resonant mode of the structure. The oscillation at 724MHz and 1.006GHz starts with ~1.6mW and ~1.9mW, and grows to -8dBm and -3dBm, respectively.

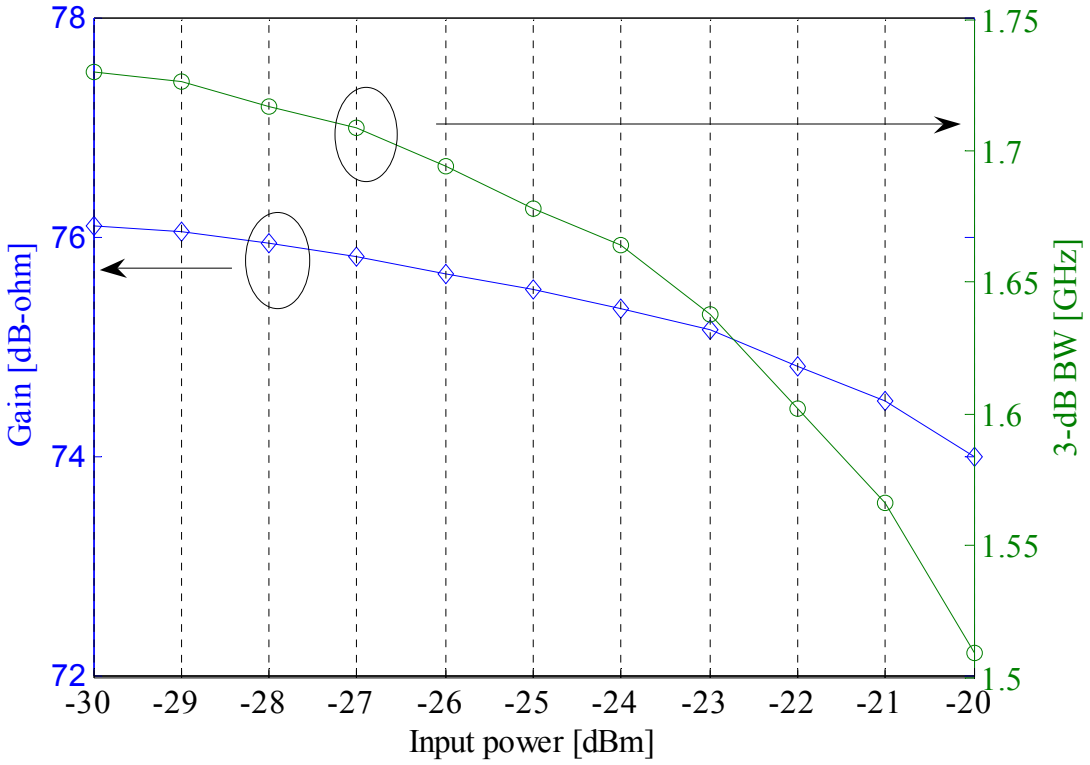


Fig. 3.41. Large-signal gain and BW behavior of the TIA (loading = 2pF)

Table 3.1. Performance comparison of the state-of-the-art CMOS TIAs

Spec	[67]	[68]	[69]	[70]	This work
Gain (dBΩ)	64	87	82 (simulated)	61	76
BW (GHz)	2	7.6	2.4	7.2	2.5
C_{in} (pF)	0.1	0.15	1	0.25	0.5
Dynamic range (dB)	124	N/A	66	N/A	138
Input-referred noise (pA/√Hz)	4.2	N/A	19 (simulated) @1GHz	8.2	<7 (0.1-0.9GHz)
GBW/P_{DC} (GHz.Ω/mW)	296	1001	1549	115	2190
P_{DC} (mW)	10.7	170	19.5	70.2	7.2
Chip area (mm^2)	0.34	1.83	0.07	0.14	0.33
Process	0.18µm BiCMOS*	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS

The phase-noise measurement is measured at V_{DD}=1.5V. Owing to its higher Q, the phase-noise of 1.006GHz oscillator reaches −94dBc/Hz at 1kHz offset and outperforms the 724MHz oscillator by 8-12dB (Fig. 3.42). Higher TIA noise at 1.006GHz partially offsets its higher output power, resulting in ~2dB improvement in phase-noise floor, -154dBc/Hz. In comparison with previously reported state-of-the-art AlN-on-Si oscillators [7], improvement in phase-noise floor is due to the lower noise TIA. Fig. 3.43 shows the micrograph of the die fabricated in 0.18µm 1P6M CMOS process when interfaced with the 724MHz AlN-on-Si resonator. The resonator dimensions are less than 300µm×100µm. The absence of on-chip inductors has reduced the IC area to 650µm×500µm.

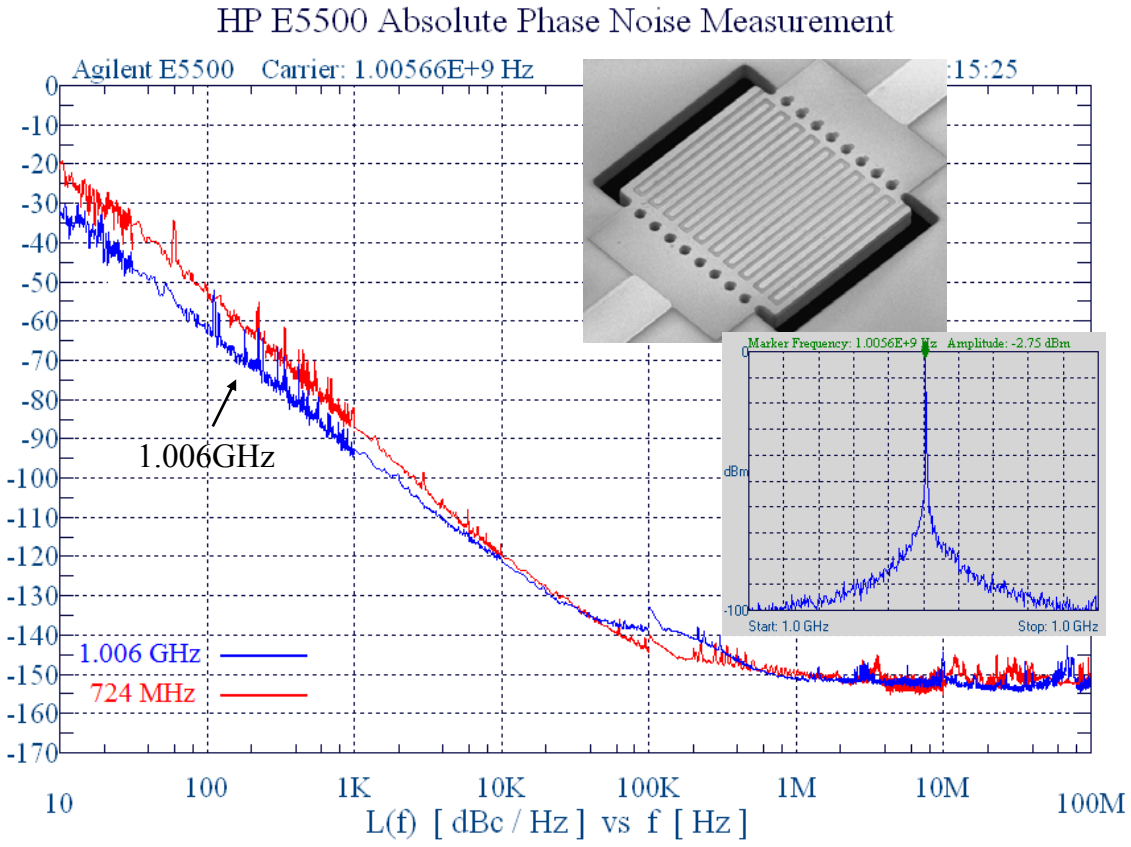


Fig. 3.42. Measured output spectrum and phase-noise of 1.006GHz oscillator

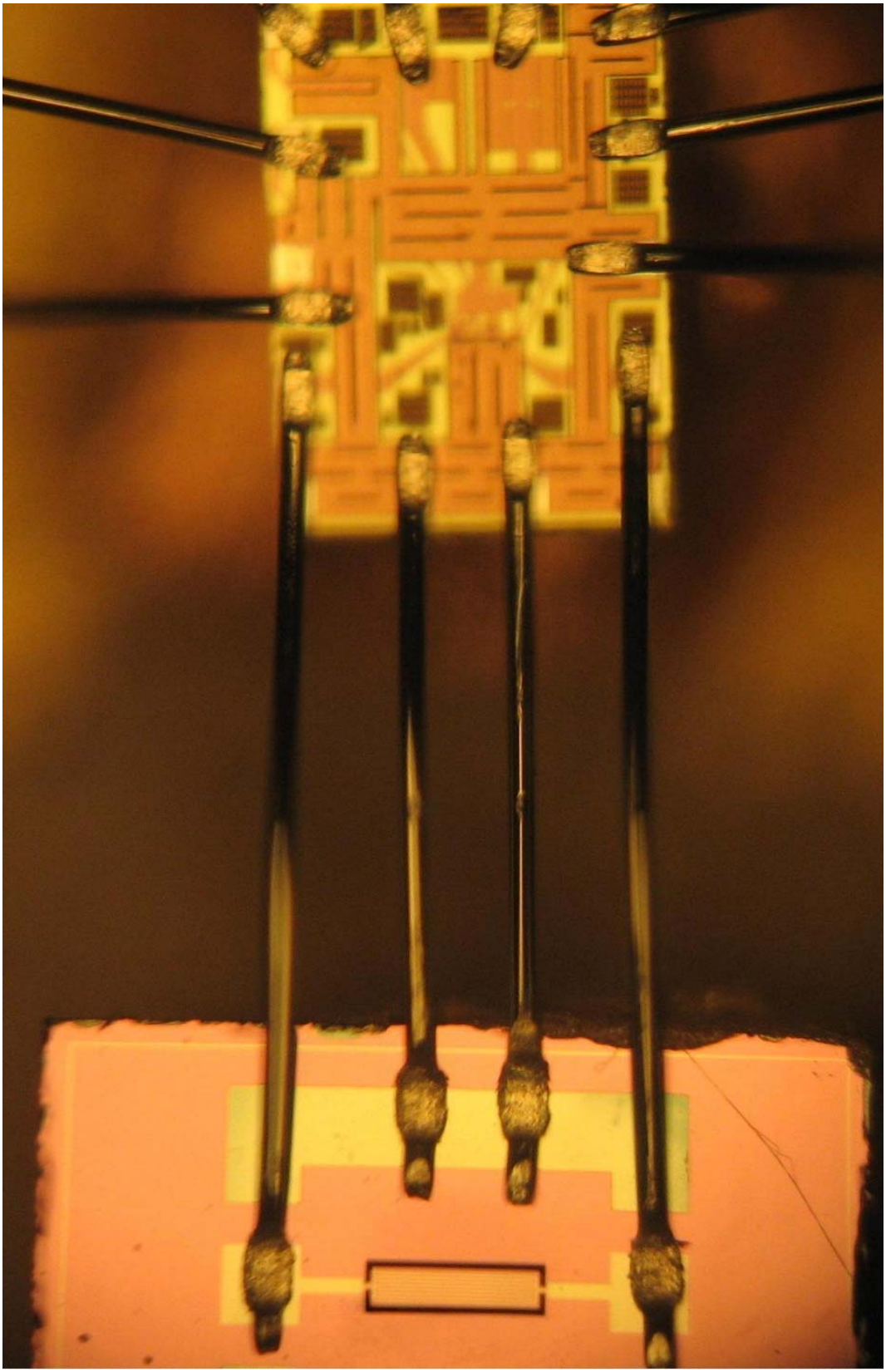


Fig. 3.43. Micrograph of the IC when interfaced with the 724MHz resonator

3.6.6 Comparison of Different Enhancement Techniques

Comparing the enhancement techniques presented in previous sections reveals that the best approach to reduce the input-referred noise and provide good noise matching is to use shunt-shunt feedback at the input of the TIA. The shunt-shunt feedback also helps increase the BW. The gain enhancement at low power consumption is best achieved when a current pre-amplifier is used in addition to the current-to-voltage conversion stage. Pole cancellation is the key to improve the BW without sacrificing the gain and having to resort to the unpleasant choice of increasing the power consumption. Another valid concern is the linearity of the TIA that is best achieved with feedback TIA configuration. Table 3.2 summarizes the comparison of different TIA techniques.

Table 3.2. Comparison of different high performance techniques

Topology	Gain	BW	Noise	Linearity	Power
Multi-stage feedback	4	5	3	1	5
Inverter TIA	2	4	2	2	3
Regulated Cascode	5	2	4	4	2
Feedback with inductive peaking	3	3	3	3	4
Current-based w/ feedback	1	1	1	3	1

3.7 Conclusion

Stringent gain, noise, BW, and power consumption requirements for the TIAs that are used as sustaining amplifier of micromechanical oscillators call for a modified for the high frequency low-power TIA design. In this chapter, a systematic approach to the design of open-loop and feedback TIAs for lateral micromechanical oscillators along with performance improvement techniques are presented.

CHAPTER 4: Electronic Tuning for Lateral MEMS Oscillators

Frequency tuning is an integral part of any micromechanical reference oscillator as it provides a mechanism to compensate for process and temperature variation in the reference oscillator [22]. In addition, for sufficiently large tuning range, it increases the functionality of radio transceivers by covering several channels that fall into the frequency tuning range.

This chapter explores electronic frequency tuning for lateral micromechanical oscillators. The discussion starts with introduction into different frequency tuning methods for micromechanical oscillators and continues on electronic tuning techniques for series-resonant micromechanical oscillators. Then, the effect of resonator parasitic is investigated to determine the practical limits for the frequency tuning range in lateral series-resonant micromechanical resonators. Next section presents tuning enhancement methods based on parasitic cancellation and offers examples from tunable high frequency lateral micromechanical oscillators to support and benchmark the performance of oscillators for each method.

4.1 Introduction

The ability to tune the frequency of oscillation is a key requirement to achieve accurate and temperature/process-compensated reference oscillator. The frequency tuning in micromechanical oscillators is either achieved by varying the resonance frequency of micromechanical resonator or by introducing additional phase-shift in the oscillation loop (mainly on the sustaining amplifier side). Several techniques have been used to tune the

frequency of micromechanical resonators. These techniques can be categorized into two groups: resonator-based techniques and electronic-based techniques.

Resonator-based techniques rely on the acoustic properties of the resonator structure to induce a shift in the resonance frequency. Since the mechanical resonance frequency is proportional to $K_{electrical}/K_{mechanical}$, the mechanical resonance frequency of a fixed geometry can be changed either through electrostatic tuning or mechanical/material tuning methods. Electrostatic tuning involves the use of an electrical signal to vary $K_{electrical}$ in a predictable manner. Flexural beam resonators or IBAR take advantage of this method to deliver significant tuning range in excess of 1000ppm.

Mechanical/material tuning is more complicated. Permanent shift in the resonance frequency can come through mass loading [71] or excessive doping [72]. Temporary shift in the resonance frequency can be achieved by exploiting the dependency of Young's Modulus to parameters such as temperature [6]. Both of electrostatic and mechanical/material tuning techniques require large DC voltages and increase the power consumption of the system. Moreover, the absence of polarization voltage makes these methods impractical for piezoelectric resonators.

Electronic frequency tuning techniques for micromechanical resonators primarily rely on creating a phase-shift in the oscillation loop. This phase-shift is usually achieved by using a tunable capacitor or a varactor whose capacitance can be independently controlled by an electrical signal. Depending on the type of the resonator and the required tuning range,

the tunable capacitor can be placed either in series or in parallel with the micromechanical resonator. Parallel tuning has been used extensively for temperature compensation in quartz crystal oscillators to deliver voltage-controlled crystal oscillators (VCXO). Series tuning is a natural choice for series-resonant micromechanical oscillators; however, it is yet to be fully explored as a viable alternative that can provide large tuning range that is sufficient to tackle the complicated process and temperature compensations of these reference oscillators. The goal of this study is to identify the limitations of series tuning technique and find ways to address these shortcomings.

4.2 Electronic Tuning for Series-Resonant Micromechanical Oscillators

Series-resonant micromechanical resonators can benefit from both parallel and series tuning. Series-resonant micromechanical resonators can be categorized into two groups: thickness-mode and lateral-mode micromechanical resonators. Although both types of series-resonant micromechanical resonators can benefit from parallel and series tuning, the focus of this work is on lateral-mode micromechanical resonators with large shunt parasitic capacitance.

4.2.1 Parallel Tuning

Parallel tuning can be accomplished either by adding a feedthrough tunable capacitor between the input and output terminals or by adding a shunt tunable capacitor between the input/output terminal and reference ground. Changing the feedthrough capacitance shifts the anti-resonance frequency of the resonator which in turn, pulls the resonator away from the natural resonance frequency. The amount of tuning is dependent on the resonator feedthrough capacitance, initial value of the tunable capacitor, and its tuning range. This approach is more effective for thickness-mode series-resonant

micromechanical resonators where the feedthrough capacitance is large and has a measureable impact on the resonance frequency. Changing the effective feedthrough capacitance of FBAR that has negligible shunt parasitic capacitance has the potential to deliver large tuning range in excess of 10000ppm. On the other hand, for lateral-mode series-resonant micromechanical resonators with very small feedthrough capacitance (<100fF), large shunt parasitic capacitance (>2pF) and high loss (>100Ω), this approach is not very effective. For these micromechanical resonators, the recommended approach is to shift the resonance frequency by varying the shunt parasitic capacitance of the resonator. This approach has been widely used in VCXOs for frequency pulling in the order of few hundred ppm. For higher-loss micromechanical resonators, the tuning is even smaller.

Several oscillator topologies are suitable for parallel tuning. A universal topology that is widely used for both quartz crystal and micromechanical oscillators is the Pierce topology (Fig. 4.1). In Pierce oscillator, the oscillation criteria is satisfied slightly off-resonance which is due to the influence of shunt capacitors at the input and output of the sustaining amplifier. At oscillation, the resonator exhibits inductive behavior and exhibits near 90º phase shift. Additional phase-shift comes from the inverting amplifier (180º) and shunt capacitors (90º). The oscillation frequency can be determined by equation (4.1). The major problem with Pierce oscillator topology is the close-to-carrier phase-noise performance; the effective Q of the resonator when operates off-resonance is significantly lower. This gives rise to higher phase-noise which is undesirable. Another important

problem is the limited tuning range (<500ppm) for high-frequency lateral micromechanical resonators with high Q and small motional capacitance.

$$\omega_0 \approx \frac{1}{\sqrt{L_{eq}\left(C_{p1} \parallel C_{p2}\right)}} \approx \frac{1}{\sqrt{L_{eq}\left(C_{p1}+C_{p2}\right)}}$$

$$A_{loop} \approx \left(g_m + g_{mb}\right) R_{loop} \frac{C_{p2}}{C_{p1}}$$

$$R_{loop} \approx R_f \left[r_{o,n} \parallel r_{o,p} \parallel \left(\frac{X_2^2}{R_m}\right) \parallel \left(\frac{X_2^2}{X_{eq}^2}\right) \right] \quad . \tag{4.1}$$

$$X_2 = \frac{1}{\omega_0 C_{p2}}$$

$$X_{eq} = \frac{1}{\omega_0} \frac{C_{p1}+C_{p2}}{C_{p1}C_{p2}}$$

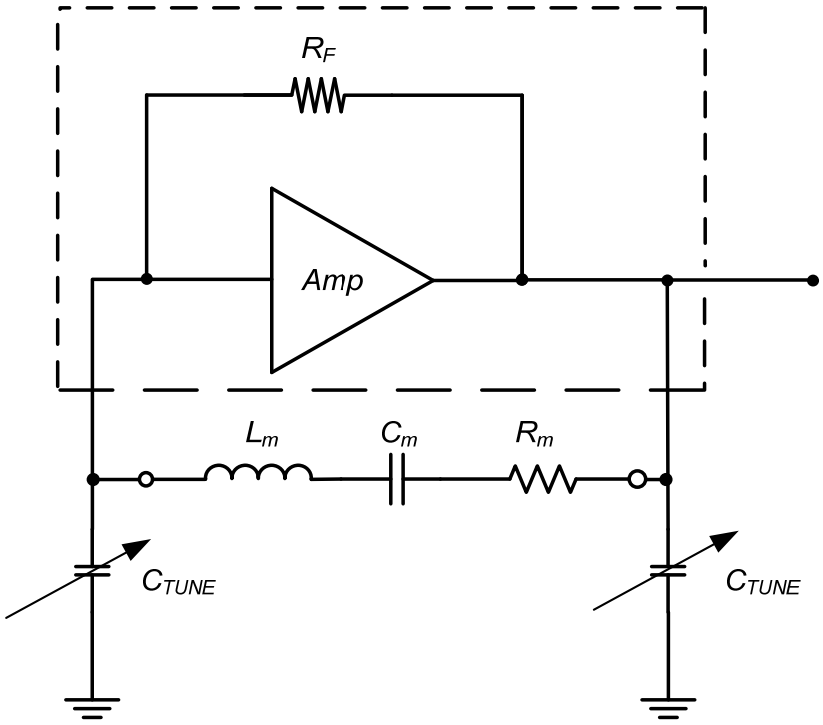


Fig. 4.1. Block diagram of a pierce oscillator

Another parallel tuning method that can be used for lateral micromechanical oscillators with large shunt parasitic capacitance is creating extra phase-shift in the loop by shifting

the frequency of one or more poles/zeros of the closed-loop system (Fig. 4.2). Exploiting the effect of large shunt parasitic capacitance on the frequency of oscillation, the extra phase-shift created in this method combined with the large gain of the TIA satisfies the oscillation condition at a frequency that is slightly different from the resonance frequency of the micromechanical resonator. The main concern in this tuning method is that the TIA needs to have large excessive gain beyond what is needed to satisfy the oscillation gain criterion. Similar to the Pierce oscillator, this method results in lower effective Q when the oscillation is sustained. This lower Q results in inferior phase-noise performance that is undesirable for low phase-noise micromechanical oscillators. Moreover, it has a negative impact on the absolute frequency accuracy of the oscillator.

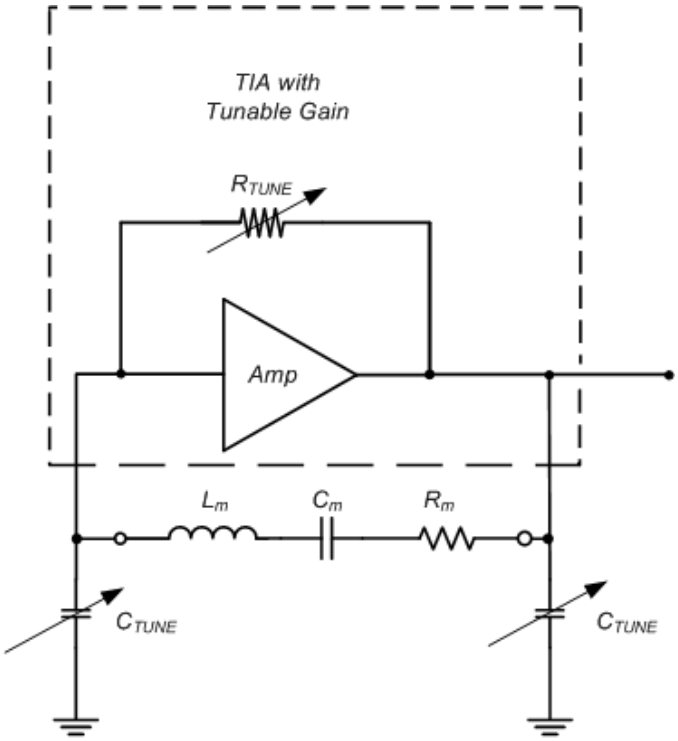


Fig. 4.2. Block diagram of the oscillator that uses parallel tuning

To demonstrate the frequency tuning range achieved with this method, a 497MHz lateral micromechanical resonator (R_m~250Ω, $Q_{unloaded}$~1,500, C_p~2.5pF) is interfaced with a

three-stage 0.18µm tunable CMOS TIA that uses cascaded feedback topology explained in 4.4.5 (Fig. 4.3). The TIA achieves maximum transimpedance gain of 72dBΩ up to 900MHz across PVT with 2pF input/output capacitive load and burns less than 24mW. Using the gain tuning that is incorporated into the first stage of the TIA the frequency of the oscillation can be varied by over 600ppm from 497.31MHz to 497.61MHz (Fig. 4.4).

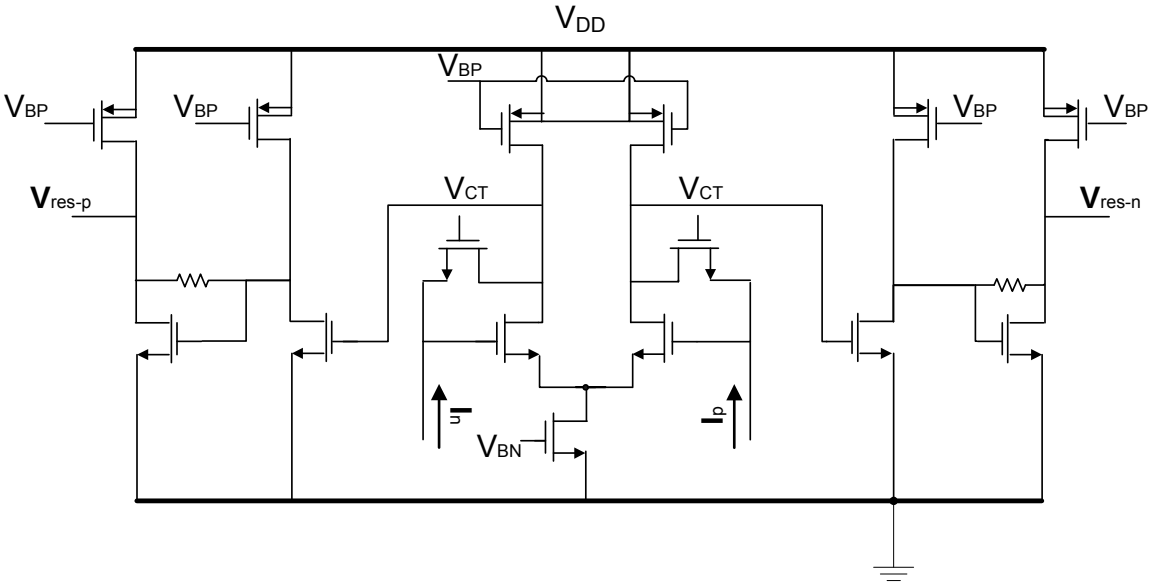


Fig. 4.3. Schematic of the three-stage CMOS tunable TIA

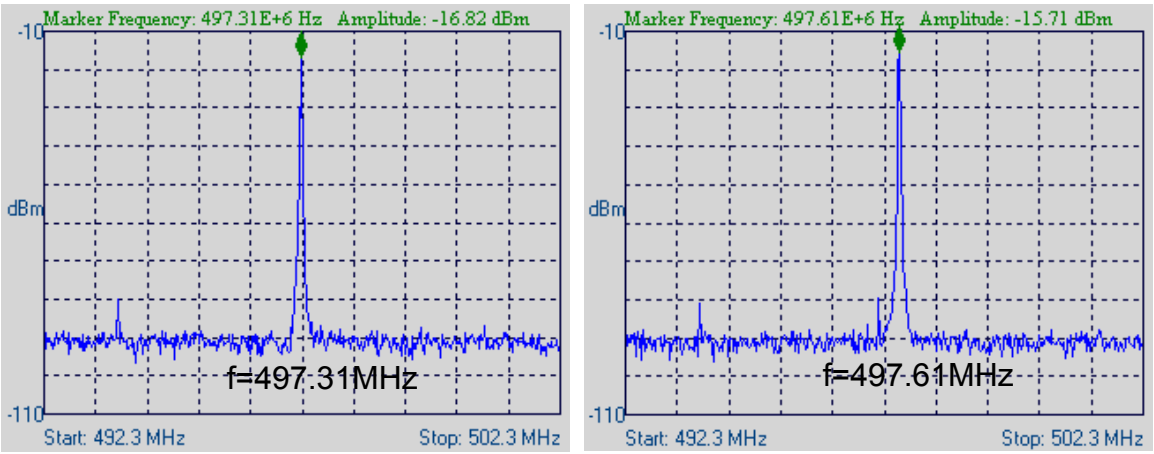


Fig. 4.4. Output spectrum of the 497MHz tunable oscillator

Although this tuning range is relatively large, the phase-noise degradation (over 10dB across the tuning range) due to Q poses a considerable challenge to successful realization

of low phase-noise tunable lateral micromechanical oscillators. The tuning range is determined by the amount of phase-shift in the loop that is in-turn proportional to the ratio of the resonator motional capacitance, C_m, to its shunt parasitic capacitance, C_p. As such, at lower frequencies, the tuning range may be comparable (>4000ppm at 27MHz).

4.2.2 Series Tuning

Series tuning is the most natural choice for series-resonant micromechanical oscillators and is usually accomplished by placing a tunable capacitor in series with the resonator in the oscillation loop that changes the effective motional capacitance of the resonator. The tunable capacitor can be placed either on the IC side, for ease of electronics design and control, or integrated with the resonator for best tuning performance (Fig. 4.5).

For oscillators that are built with series-resonant micromechanical oscillators, the series combination of varactor and motional capacitance of the resonator, C_m, exhibits lower overall capacitance, which in-turn causes an upward shift in the oscillation frequency. The amount of frequency shift can be accurately determined by designing a precision control circuitry to supply the varactor tune signal.

In oscillators that are built based on series-resonant resonators with minimal shunt parasitic such as quartz crystal or FBAR, series tuning provides large tuning range with a potential to offer a fully-electronic temperature- and process-compensated solution. However, the designers still have to watch for the effect of large feedthrough parasitic of high frequency thickness mode resonators such as FBAR on the tuning range and phase-noise performance of the oscillator.

4.3 Series Tuning in Lateral Micromechanical Oscillators

Series tuning for lateral micromechanical oscillators warrants a more detailed study as these resonators suffer from large parasitics (especially large shunt parasitic capacitance) that have a major negative impact on the tuning range of the oscillator. In this section, the effect of parasitics on the tuning range of the oscillator is investigated.

4.3.1 Lateral Micromechanical Oscillator with Ideal Resonator

A lateral micromechanical oscillator based on an ideal series-resonant micromechanical resonator with no shunt and feedthrough parasitic capacitance, the oscillation frequency is given by:

$$f_{tune0} = \frac{1}{2\pi\sqrt{L_m\left(\frac{C_m C_{tune,0}}{C_m + C_{tune,0}}\right)}}, \tag{4.2}$$

where $C_{tune,0}$ is the minimum varactor capacitance and C_m is the motional capacitance of the micromechanical resonator. The maximum tuning range of the micromechanical oscillator can be expressed by:

$$\frac{f_{tune,1}}{f_{tune,0}} = \frac{f_{tune0} + \Delta f}{f_{tune,0}} = \sqrt{\frac{(1+k)(C_{tune,0} + C_m)}{C_m + (1+k)C_{tune,0}}} = \sqrt{1 + \frac{kC_m}{C_m + (1+k)C_{tune,0}}}, \tag{4.3}$$

where k is the varactor tuning ratio. According to (4.3), there is no theoretical upper limit to the tuning range for infinitely-large tuning ratio or infinitely-small tunable capacitor. In practice, however, the tuning range is severely limited due to the resonator parasitic, especially the large shunt parasitic capacitance appearing at the input and output of most lateral micromechanical resonators.

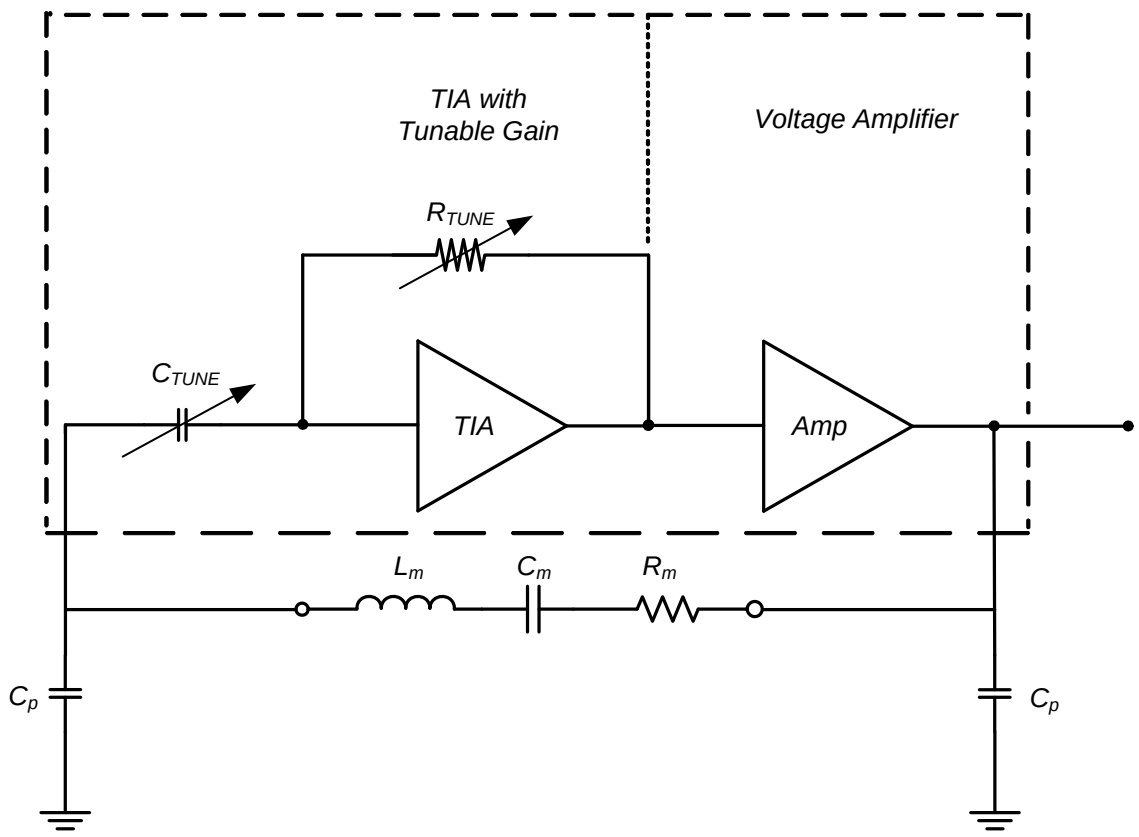


Fig. 4.5. Diagram of the tunable micromechanical oscillator that uses series tuning

4.3.2 Lateral Micromechanical Oscillator with Practical Resonator

Practically, lateral micromechanical resonators exhibit parasitic effects both in the form of feedthrough capacitance and shunt parasitic capacitance at both the input and output terminals. The feedthrough capacitance is very small (<50fF) and therefore, has a negligible effect on the tuning range of the micromechanical oscillator. Here, we focus more on the effect of shunt parasitic capacitance on the tuning range of the lateral micromechanical oscillator. For an oscillator based on a series-resonant micromechanical resonator with input/output shunt parasitic capacitance and no feedthrough parasitic, the oscillation frequency is given by:

$$f_m = \frac{1}{2\pi\sqrt{L_m C_m}}\sqrt{1+\frac{C_m\left(2C_p + C_{tune,0}\right)}{C_p\left(C_p + C_{tune,0}\right)}}, \tag{4.4}$$

where C_p is the shunt parasitic capacitance of the lateral micromechanical resonator. Using equation (4.4), the maximum tuning range can be expressed by:

$$\frac{f_{tune,1}}{f_{tune,0}} = \sqrt{\frac{\left(C_p + C_{tune,0}\right)\left\{C_p\left[C_p + (1+k)C_{tune,0}\right] + C_m\left[2C_p + (1+k)C_{tune,0}\right]\right\}}{\left[C_p + (1+k)C_{tune,0}\right]\left[C_p\left(C_p + C_{tune,0}\right) + C_m\left(2C_p + C_{tune,0}\right)\right]}}, \tag{4.5}$$

Equation (4.5) clearly demonstrates the limitation to the maximum frequency tuning range in the presence of resonator shunt parasitic capacitance; the maximum tuning range is inversely proportional to the ratio of C_p over C_m. For an infinitely-small varactor ($C_{tune,0} \ll C_m \ll C_p$), the maximum tuning range can be approximated by:

$$\frac{f_{tune,1}}{f_{tune,0}} \approx \sqrt{1+\frac{2C_m}{\left[C_p + (1+k)C_{tune,0}\right]}}. \tag{4.6}$$

Often times, in practical applications with on-chip electronic tuning, the choice of process technology determine the minimum available size of the on-chip varactor. To have an idea about what would be the maximum tuning range in this case, a 500MHz micromechanical resonator with $Q_{unloaded}$=2,000, R_m=200Ω, and C_p=2pF is considered. Equation (4.6) gives around 3000ppm for maximum tuning range. However, unless using a deep sub-μm process with nanometer range feature size, the minimum value of the varactor, $C_{tune,0}$, is at least an order of magnitude higher than C_m of the micromechanical resonator. In this case, the maximum tuning range can be approximated by:

$$\frac{f_{tune,1}}{f_{tune,0}} \approx \sqrt{\frac{C_p}{C_p + C_m} + \frac{2C_m}{C_p + 2C_m}}. \tag{4.7}$$

In this case, the maximum tuning range of the same 500MHz micromechanical oscillator drops below 500ppm which is simply not sufficient for most process and temperature

compensation applications. In order to better understand the challenges posed to the oscillator tuning by the shut parasitic capacitance of the resonator, the frequency tuning of the same 500MHz oscillator is plotted vs. the shunt parasitic capacitance, C_p for different Q and R_m values (Fig. 4.6). Each plot has a family of curves for different resonator Q with a fixed R_m. The study of these curves shows that the frequency tuning range severely deteriorates when the shunt capacitance is increased beyond 1pF. In fact, even for very small shunt parasitic capacitances in the range of 500fF, the tuning range improvement for resonators with $R_m > 200\Omega$ is relatively modest and in no way impressive (<1000ppm). What makes the matter worse is that R_m is inversely proportional with the Q; i.e. the tuning range is further shrunk for a lower phase-noise oscillator that is using a higher Q resonator. From these results it becomes clear that efforts need to be made to eliminate or at least significantly reduce the effect of shunt parasitic capacitance on the tuning range of the oscillator.

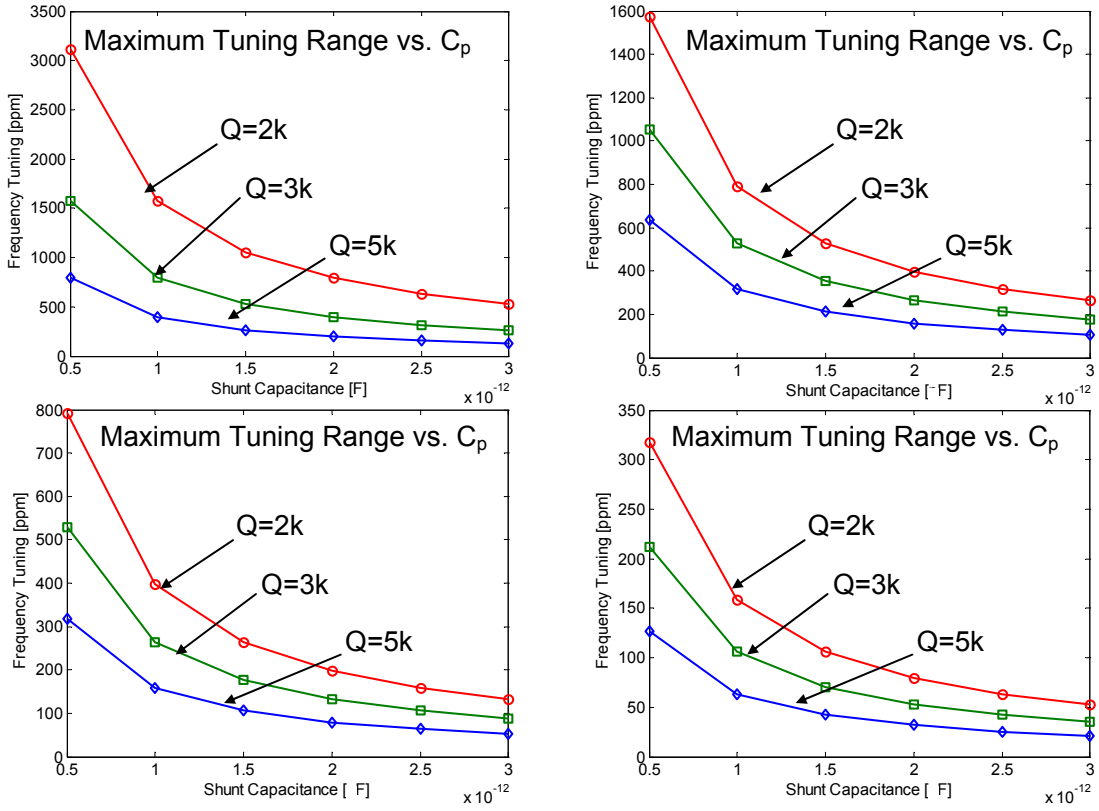


Fig. 4.6. Series tuning limitation for 500MHz lateral micromechanical oscillator

4.3.3 2nd-Order Parasitic Effects on Tuning Range

Apart from the shunt parasitic capacitance, other parasitics of the micromechanical resonators have an impact on the tuning range. Although the scope and extent of this impact is heavily dependent on the TIA topology and resonator characteristic (resonance frequency, shunt parasitic capacitance, loss, and Q), the impact from 2nd-order resonator parasitics is relatively insignificant when compared to non-idealities of the sustaining amplifier and electronic tuning network. Nevertheless the 2nd-order parasitic both from IC and micromechanical resonator continue to pose a challenge. The 2nd-order parasitic effects in the resonators mostly include the feedthrough capacitance. The effect of

feedthrough capacitance on the resonator is usually negligible as the varactor capacitance, $C_{tune,0}$, is significantly larger than the feedthrough capacitance.

2^{nd}-order effects from the electronics are centered on the nonlinearity of the varactor. These nonlinearities include Q limitation, self-resonance, noise, and the dynamic range.

Low-Q varactors cause degradation in phase-noise performance by adding to the overall noise of the sustaining amplifier. In addition, they negatively affect the tuning range by adding a series parasitic resistance. This extra resistance limits the effective capacitance change across the tuning range which results in smaller tuning range.

Limited self-resonance frequency for the varactor can be modeled by a series inductor. Similar to the Q limitation this effect results in smaller change in varactor capacitance across the tuning range with negative consequence for the tuning range.

Noise of the varactor is a critical issue in the performance of the oscillator. Although it may not have a direct impact on the tuning range of the micromechanical oscillator, its effect on the phase-noise degradation can not be ignored. The main noise sources for MOS and junction varactor are flicker and thermal. These noise sources contribute to the phase-noise of the oscillator with the former having a major impact on the close-to-carrier phase-noise performance. The specified phase-noise requirement for the micromechanical reference oscillator may indirectly limit the useful tuning range.

Dynamic range limitation is a significant challenge for any electronic circuit operating in large-signal regime. Oscillators that benefit from high-gain TIAs are no exception. The dynamic range of the varactor further constrains the performance of the oscillator by reducing the spurious-free dynamic range (SFDR) that results in severe degradation in phase-noise performance (especially far-from-carrier). This could be in the form of higher power harmonics, i.e. larger total harmonic distortion (THD) content with impact on the far-from-carrier phase-noise, and/or the appearance of unwanted spurs in the phase-noise of the oscillator. Similar to varactor noise, the outcome may indirectly affect the usable tuning range of the micromechanical reference oscillator.

4.4 Tuning Range Enhancement through Shunt Capacitance Cancellation

From the discussion in section 4.3, it is now obvious that the tuning range in high frequency lateral micromechanical oscillators are significantly limited by the presence of shunt parasitic capacitance to a level that is not sufficient for the majority of applications. Naturally, the tuning enhancement techniques have to focus on this issue by trying to reduce (and hopefully completely cancel) the effect of shunt parasitic capacitance of the resonator on the oscillator tuning range. Therefore capacitance cancellation techniques become necessary. This section focuses on different approaches for cancelling the shunt parasitic capacitance of the resonator.

4.4.1 Active Inductance Cancellation

A well-known approach to cancel the effect of an electrical circuit element is to use its dual counterpart to cancel its effect. In this case, the shunt parasitic capacitance can be resonated out at or near the frequency of oscillation with an appropriately-sized inductor (Fig. 4.7). Due to the low frequency of oscillation in majority of cases (<1GHz), the

inductance value is relatively large (>20nH). Monolithic on-chip inductors are very low-Q and consume large on-chip area. In addition, they can not be tuned to accommodate for the possible variation in the effective shunt parasitic capacitance that is usually present in practical applications (e.g. bondwire and IC parasitic). Therefore, they are not a good choice for shunt parasitic cancellation. On the other hand, active inductors are relatively small, tunable and potentially exhibit higher Q [49], [62].

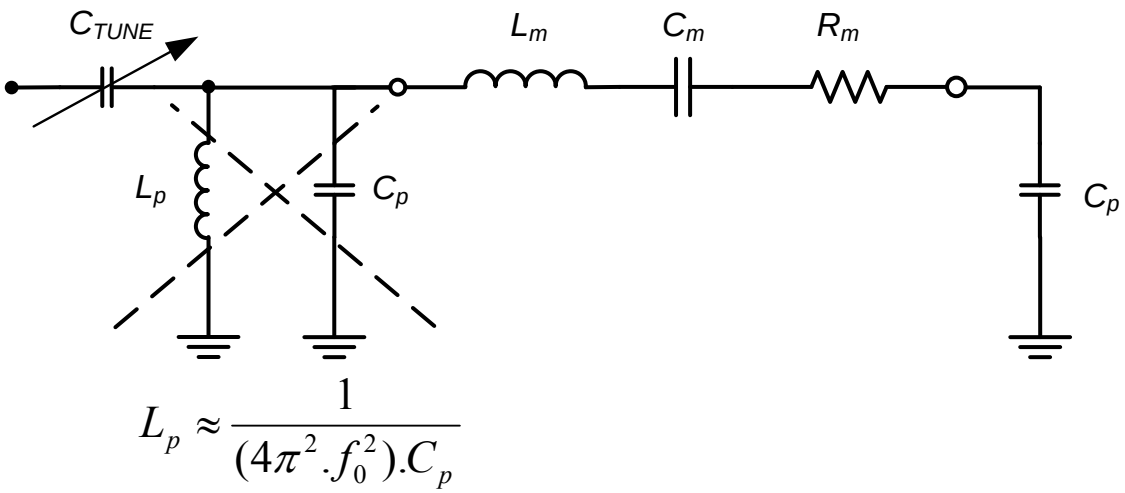


Fig. 4.7. Concept of tuning enhancement based on active inductor cancellation

The main disadvantage of active inductors when compared to their passive counterparts is the excessive noise associated with the active elements used in the active inductor. The higher noise calls for minimizing the number of active elements. A single-transistor one-port active inductor that is a derived from common drain (CD) topology can potentially result in minimal extra noise at the expense of smaller tuning range [49]. Fig. 4.8 shows the schematic of the single-transistor one-port active inductor with its equivalent lumped electrical circuit model.

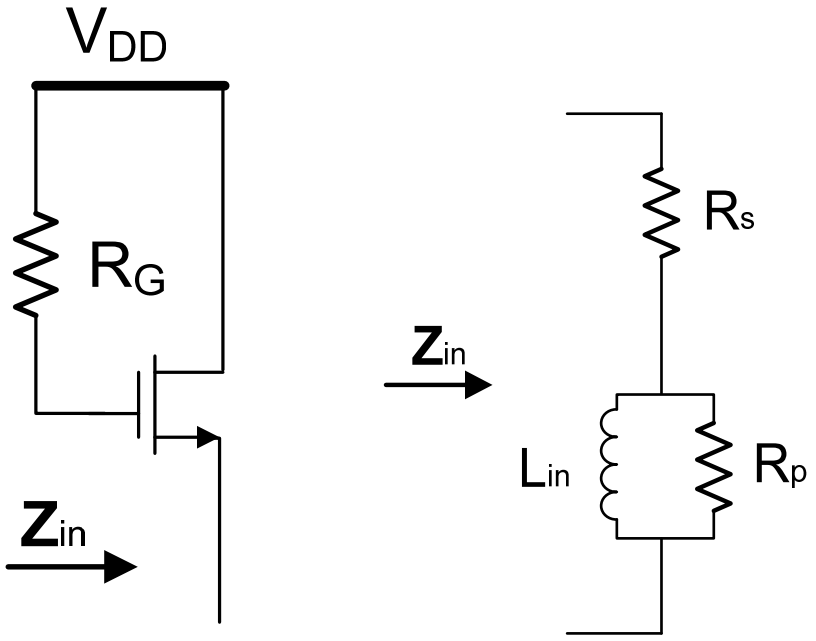


Fig. 4.8. Schematic and equivalent model of the single-transistor active inductor

The input impedance of the circuit can be expressed by:

$$Z_{in} \approx \frac{R_G C_{gs}.s+1}{g_m + C_{gs}.s}$$
$$Z_{in}\big|_{s\to 0} \approx \frac{1}{g_m} \quad , \tag{4.8}$$
$$Z_{in}\big|_{s\to \infty} \approx R_G$$

where g_m and C_{gs} are the transconductance and gate-source capacitance of the MOS transistor. The input resistance approaches a purely resistive value at very low and very high frequencies that are different, effectively paving the way for emulating an inductive response at a pre-defined frequency range. The equivalent inductance, L_{in} can be approximated by:

$$L_{in} = C_{gs} R_s R_p$$
$$R_p = R_G - \frac{1}{g_m}. \tag{4.9}$$
$$R_s = \frac{1}{g_m}$$

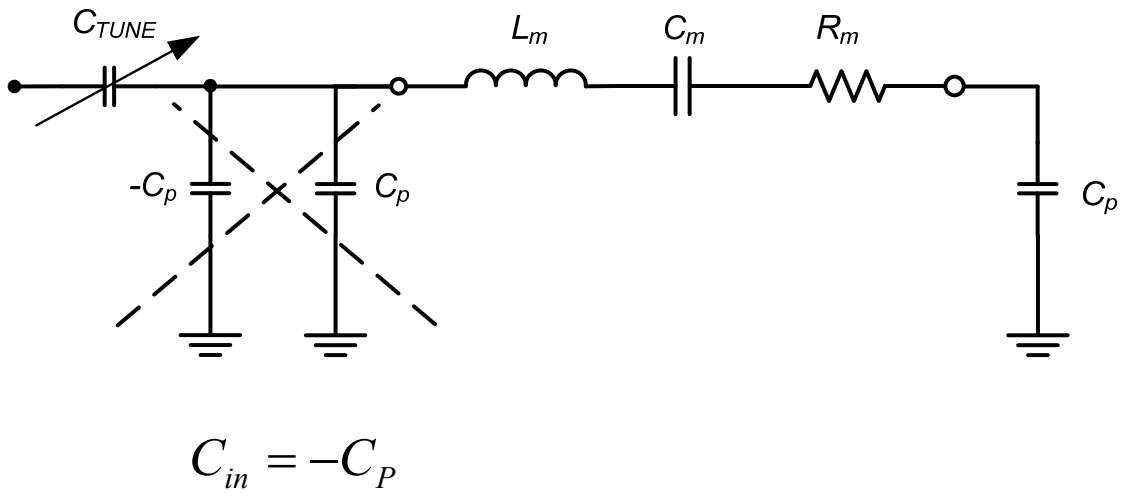
Using the information provided in equation for (4.9) for R_s and R_p, the Q of the inductor when $R_G >> 1/g_m$, can be approximated by:

$$Q_{in} \approx \frac{R_p}{L_{in}\omega} = \frac{g_m}{C_{gs}}, \tag{4.10}$$

where ω is the angular frequency. Since g_m/C_{gs} is proportional to the transition frequency (f_T) of the process, Q_{ind} is limited by the choice of process technology (transistor size) and the power consumption (transconductance). Therefore, in a given technology, a higher Q active inductor is only achieved at the expense of higher power consumption. In this work, we primarily use 0.18μm CMOS process that offers $f_T \approx 55$GHz. As such, the $Q_{ind} > 50$ may be achieved for 300MHz < ω < 1GHz. This Q is sufficient for cancelling the C_p to within 10% of its nominal value.

4.4.2 Negative Capacitance Cancellation

Another approach to cancel the shunt parasitic capacitance of the micromechanical resonator is to place a negative capacitor of equal value in parallel with the shunt parasitic capacitance at the input/output of the resonator (Fig. 4.9). For complete cancellation and best phase-noise performance, this single-port negative capacitor should be tunable, low-noise, and high Q. Meeting all of these requirements with low power consumption is challenging.



$$C_{in} = -C_P$$

Fig. 4.9. Concept of tuning enhancement based on negative capacitance cancellation

There are several methods to create a negative capacitance. Most of these methods rely on the concept of negative impedance converter (NIC). NIC usually involves an amplification stage configured in such a way to introduce a phase-shift of -180° between the voltage and current of the input signal. An NIC circuit can be used to transform any arbitrary impedance into its algebraic negative (Fig. 4.10). NIC's can be realized either as a two-port topology (with differential operation capability) such as cross-coupled pair [73] or single-port proposed by Linvill [74]. Some topologies allow for inclusion of floating nodes that make the design robust for both single- and two-port applications [74].

In this work, we use a simple two-transistor NIC that has the potential to operate both as a single-port or two-port network [74]. The original circuit is proposed by Linvill in 1953 but uses bipolar transistors. The circuit is modified for CMOS by providing current source to feed the current and a resistive network to bias the gate of the transistors. This extra resistive biasing network provides flexibility in the design as the transistor biasing is not dependent on the multiplication ratio that is required for negative capacitance

generation (Fig. 4.11). A moderate level of tuning may be required on the load capacitance, C_L, for complete cancellation.

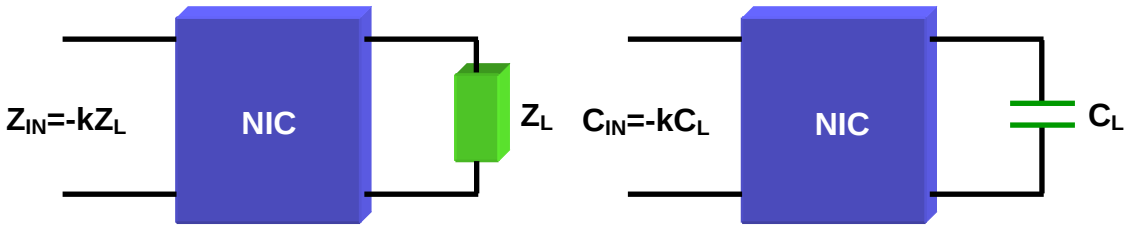


Fig. 4.10. Concept of negative impedance converter (NIC)

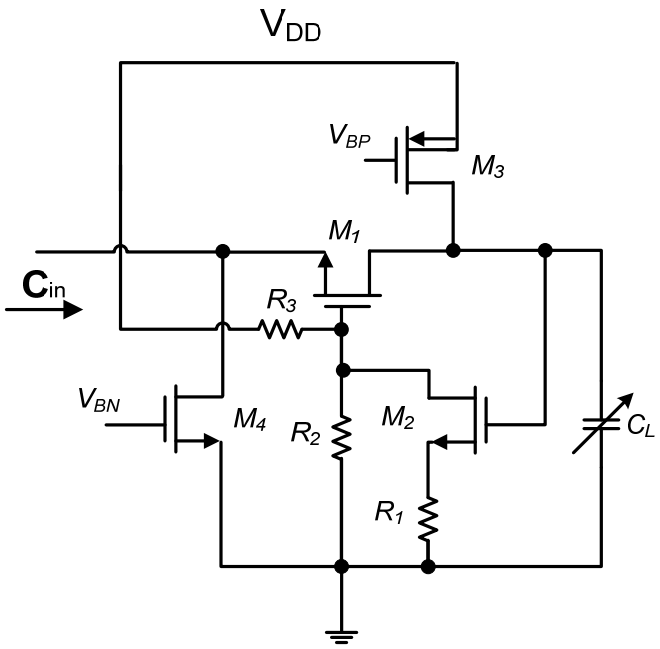


Fig. 4.11. Schematic of the single-port negative impedance generator

Fig. 4.12 shows the simplified equivalent electrical circuit for the single-port negative capacitance generator. R_2 in the electrical model is the equivalent shunt resistance from R_2 and R_3 shown in the circuit. The M_{n1} and M_{n2} devices are replaced with M_1 and M_2 in the electrical model, respectively.

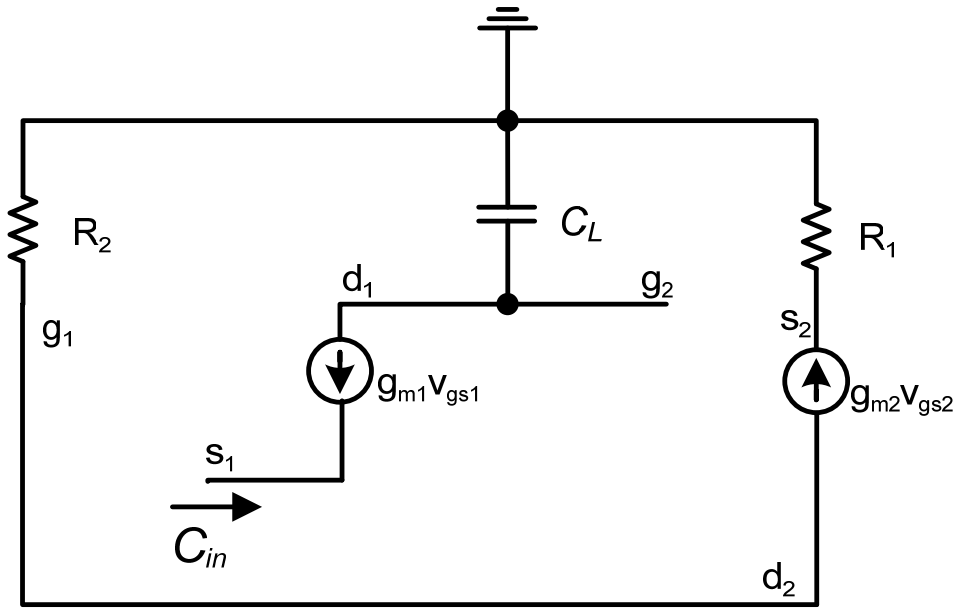


Fig. 4.12. Electrical model of the single-port negative capacitance generator

Solving for C_{in}, we have:

$$\frac{v_{g1}}{R_2} = -g_{m2}.v_{gs2} \rightarrow (1)$$

$$i_x = -g_{m1}.v_{gs1} \rightarrow (2)$$

$$v_{s2} = g_{m2}.v_{gs2}.R_1 \rightarrow (3)$$

$$v_{g2} = v_{d1} = -\frac{1}{C.s}.g_{m1}.v_{gs1} \rightarrow (4)$$

$$v_x = v_{s1} \rightarrow (5)$$

$$v_{s1} = v_{g1} - v_{gs1} \rightarrow (6)$$

$$Z_{in} = \frac{v_x}{i_x} = ?$$

$$(3),(4) \Rightarrow v_{gs1} = -\frac{C.s.(1+g_{m2}.R_1)}{g_{m1}}.v_{gs2} \rightarrow (7)$$

$$(1),(6) \Rightarrow v_x = -R_2.g_{m2}.v_{gs2} + \frac{C.s.(1+g_{m2}.R_1)}{g_{m1}}.v_{gs2} \rightarrow (8)$$

$$(2),(7) \Rightarrow i_x = C.s.(1+g_{m2}.R_1).v_{gs2} \rightarrow (9)$$

$$\frac{(8)}{(9)} \Rightarrow Z_{in} = \frac{-R_2.g_{m2} + \frac{C.s.(1+g_{m2}.R_1)}{g_{m1}}}{C.s.(1+g_{m2}.R_1)} \rightarrow (10)$$

$$\Rightarrow C_{in} = -\frac{(1+g_{m2}.R_1)}{R_2.g_{m2}}.C$$

$$\Rightarrow R_{series} = \frac{1}{g_{m1}}$$

where g_{m1} and g_{m2} are the transconductance of M_1 and M_2 devices, respectively. This analysis shows that for $g_{m1} \approx g_{m2} \approx g_m$, the input resistance, Z_{in}, can be simplified to:

$$Z_{in} = \frac{-R_2.g_m}{C_L.(1+R_1 g_m).s} + \frac{1}{g_m}, \qquad (4.11)$$

When $g_m.R_1$ is sufficiently large, i.e. $g_m.R_1>>1$, the input impedance can be further simplified to:

$$Z_{in} = \frac{-R_2}{R_1.C_L.s} + \frac{1}{g_m} \tag{4.12}$$

The real part of the input impedance, $1/g_m$, is considered the equivalent input resistance, R_{in}, of the network. Using equation (4.12), the equivalent negative capacitive can be derived as:

$$C_{in} = -\frac{(1+R_1 g_m)}{(R_2 \| R_3) g_m} C_L \approx -\frac{R_1}{(R_2 \| R_3)} C_L \tag{4.12}$$

It is clear from equation (4.12) that the equivalent negative capacitance can be independently adjusted without changing the biasing condition of transistors.

4.5 Case Studies

Three tunable oscillators are designed and fabricated in 0.18μm CMOS process to demonstrate and compare the effect of tuning enhancement techniques on the tuning range and phase-noise performance of the lateral micromechanical oscillator. All three TIA's use the same core amplifier and biasing condition with the same size varactors in series with the input to achieve the tuning. The first TIA does not use any tuning enhancement technique. The second TIA uses use active inductor cancellation while the third TIA uses negative capacitance cancellation techniques to improve the tuning range. To have a fair comparison, all three TIA's are interfaced with a 427MHz AlN-on-Silicon micromechanical oscillator (R_m~180Ω, $Q_{unloaded}$~1400, C_p~2.7pF) and the tuning range, output spectrum and phase-noise performance are monitored. The resonator frequency response is shown in Fig. 4.13.

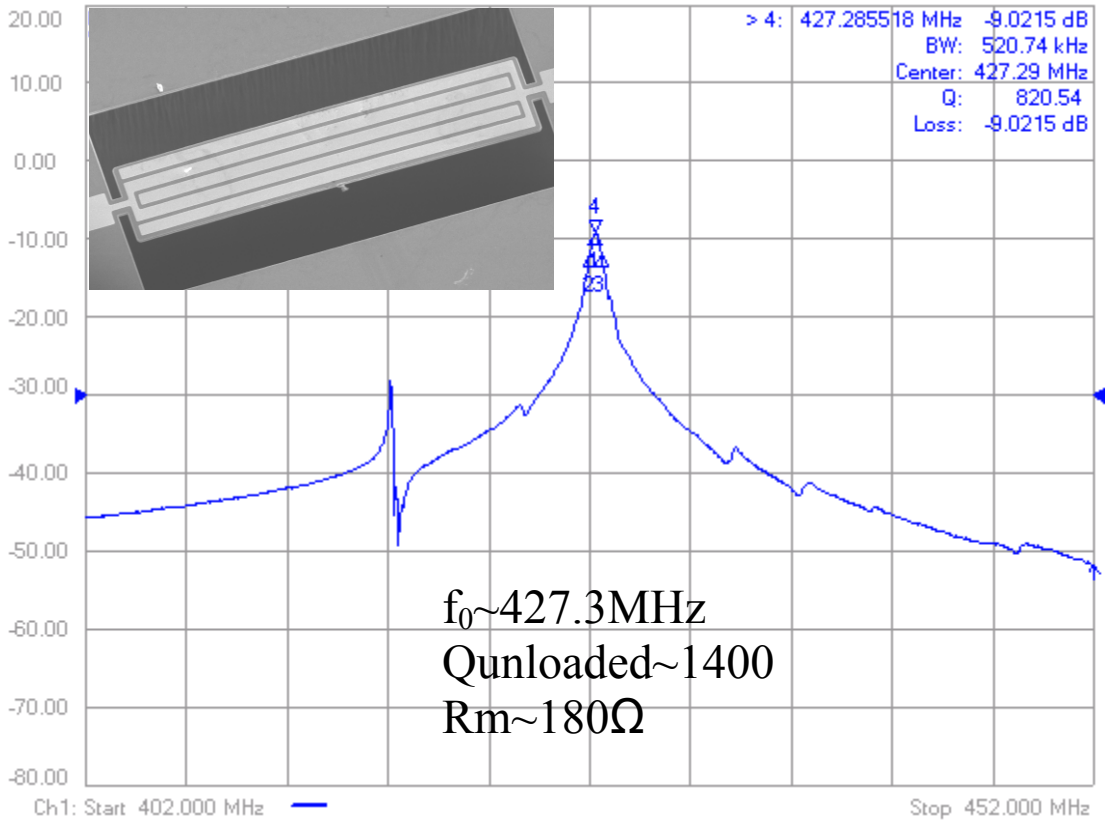


Fig. 4.13. Response and SEM view of the 427MHZ AlN-on-Si resonator

4.5.1 TIA without Tuning Enhancement

A three-stage feedback tunable TIA is designed and fabricated in 0.18μm CMOS process. The first stage is an inverter with shunt-shunt feedback and acts as the transimpedance amplification stage. The choice of inverter over CS topologies is due to the availability of larger gain. The shunt-shunt feedback is realized with an NMOS transistor biased in triode region to provide gain tuning capability. The 2^{nd} and 3^{rd} stages are voltage amplifiers that boost the gain. To lessen the effect of inter-stage critical nodes on the BW of the TIA, the last stage incorporates a local shunt-shunt feedback network to lower the input and output impedance of this stage. Together with the 2^{nd} stage, the last two stages of the amplifier form a modified Cherry-Hooper. The RC shunt-shunt feedback incorporated in the last stage is in the form a "T" network that can realize a left-hand

plane zero for pole cancellation. The tuning network is comprised of two back-to-back MOS varactors that are placed in series with the input of the TIA. This approach obviates the need for two independent tune signals and at the same time potentially lowers the minimum available tuning capacitance value (Fig. 4.14).

The TIA measures 425μm×425μm (Fig. 4.15) and consumes around 10mW and is capable of providing minimum gain above 62dBΩ up to 1.2GHz with 2pF input/output capacitive load. The gain can be tuned by ~12dB at the expense of smaller BW. The impact of the tuning network on the transimpedance gain can not be ignored. Due to the lack of shunt-parasitic cancellation, the high-pass response due to the use of small series varactors significantly lowers the gain. This effect becomes more pronounced as the varactor is tuned to the minimum capacitance in which case, the gain drops from 78dBΩ to 62dBΩ (Fig. 4.16).

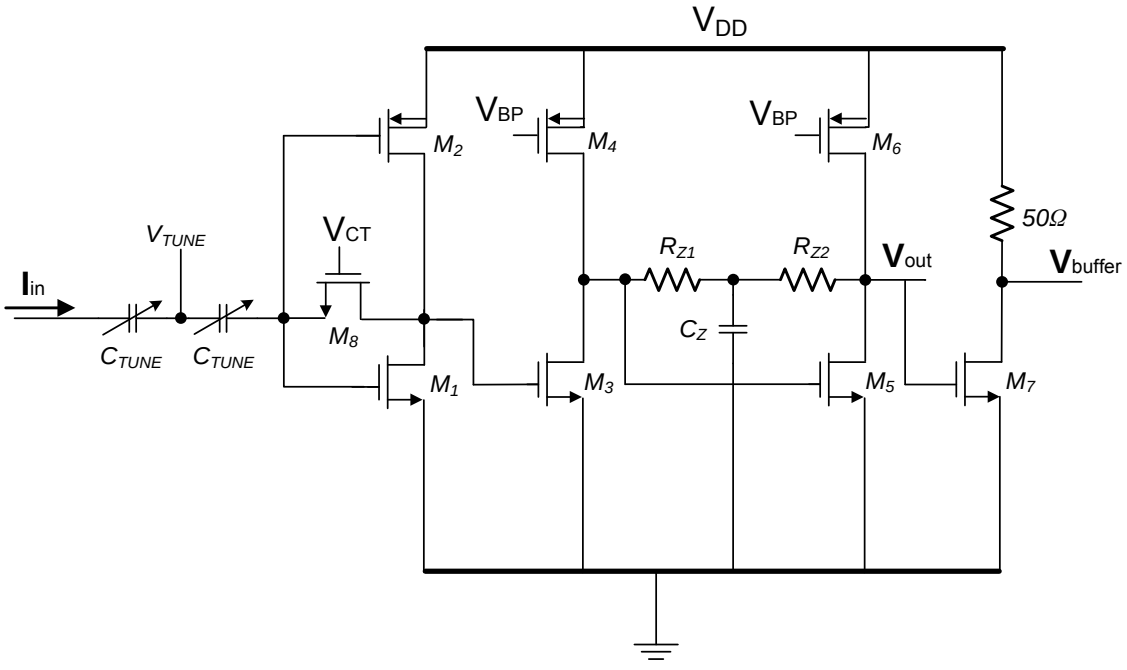


Fig. 4.14. Schematic of the tunable TIA w/o shunt parasitic cancellation

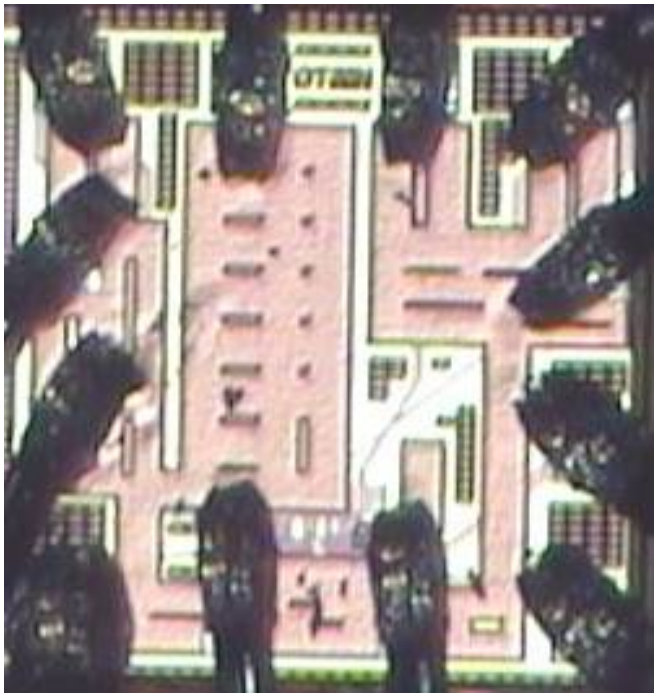


Fig. 4.15. Chip Micrograph of the TIA without shunt capacitive cancellation

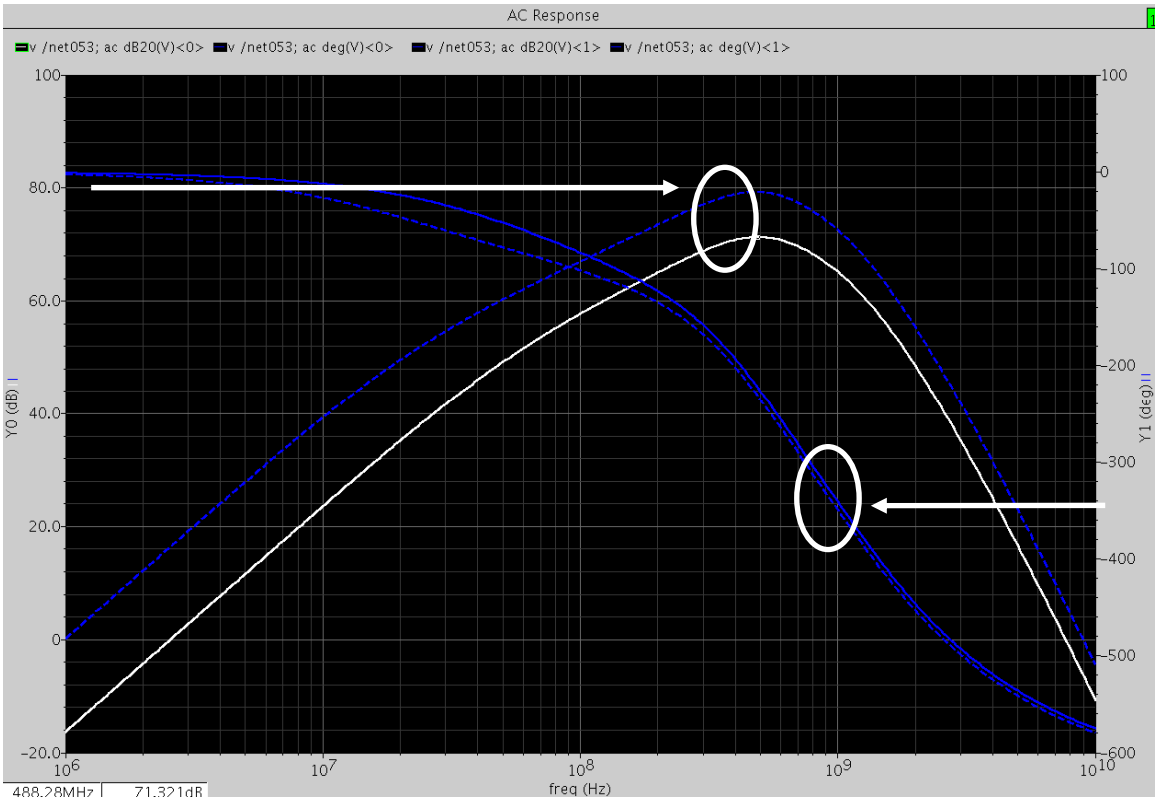


Fig. 4.16. AC gain and phase of the tunable TIA w/o shunt parasitic cancellation

The TIA is interfaced with the 427MHz AlN-on-Si lateral micromechanical resonator specified earlier in this section. The measured tuning range of the 427MHz micromechanical oscillator is around 64ppm (Fig. 4.17). This tuning range is in no way sufficient for temperature or process compensation.

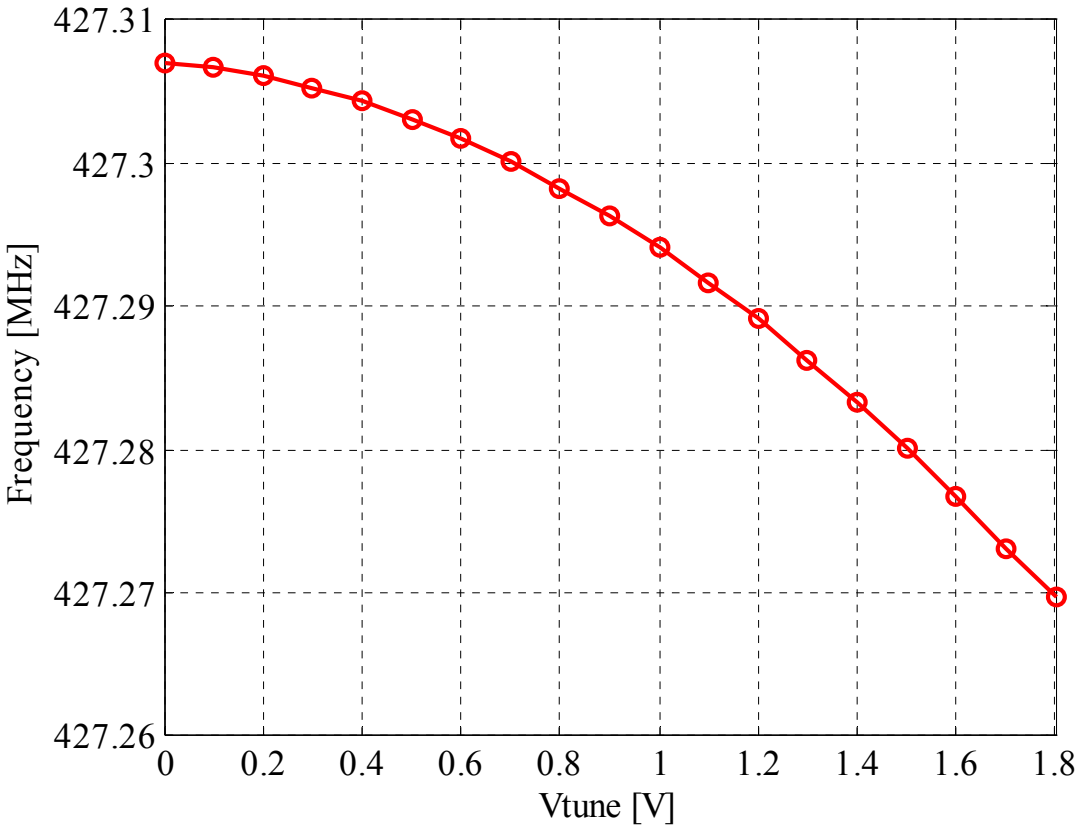


Fig. 4.17. Frequency vs. voltage for the 427MHz oscillator w/o tuning enhancement

4.5.2 TIA with Active Inductance Cancellation

A three-stage feedback tunable TIA that uses active inductor for shunt parasitc cancellation is designed and fabricated in 0.18μm CMOS process. The core amplifier is the same as the one used for oscillator without tuning enhancement. Similarly, two series back-to-back varactors that are placed at the input of the TIA play the role of tuning network. The aforementioned single-port single-transistor active inductor is added to the

input of the TIA for shunt parasitic cancellation. The bias current of the active inductor is sourced by an NMOS transistor, M_{n2}, which is connected between the ground and the input of the TIA (Fig. 4.18).

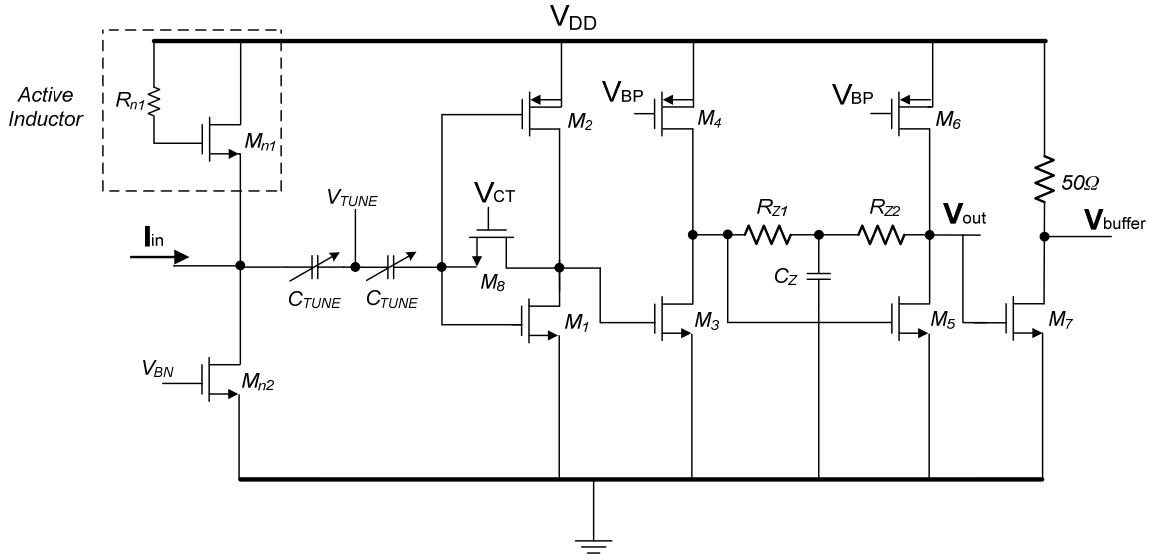


Fig. 4.18. Schematic of the tunable TIA with active inductance cancellation

The TIA measures 425µm×425µm (Fig. 4.19), consumes around 11mW, and is capable of providing minimum gain above 66dBΩ up to 1.2GHz with 2pF input/output capacitive load. The gain can be tuned by ~10dB at the expense of smaller BW. Although the impact of the tuning network on the transimpedance gain is reduced due to partial shunt parasitic cancellation, it is still considerable (>10dB) and cannot be ignored. In this case, the transimpedance gain drops from 80dBΩ to around 66dBΩ when the tuning capacitance is varied from its maximum to the minimum (Fig. 4.20).

The TIA is interfaced with the same 427MHz AlN-on-Si lateral micromechanical resonator. The measured tuning range of the 427MHz micromechanical oscillator is around 350ppm (Fig. 4.21). The tuning range, although ~5.5× larger than the oscillator

without shunt parasitic cancellation, but it is still not enough for most temperature or process compensation applications.

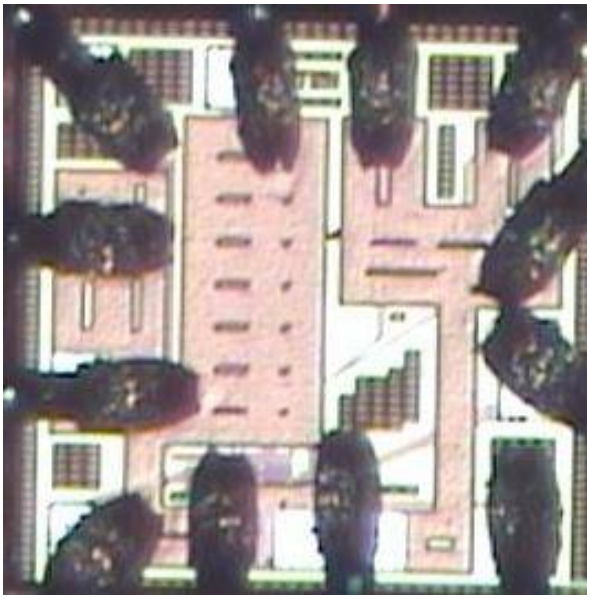


Fig. 4.19. Chip Micrograph of the TIA with active inductance cancellation

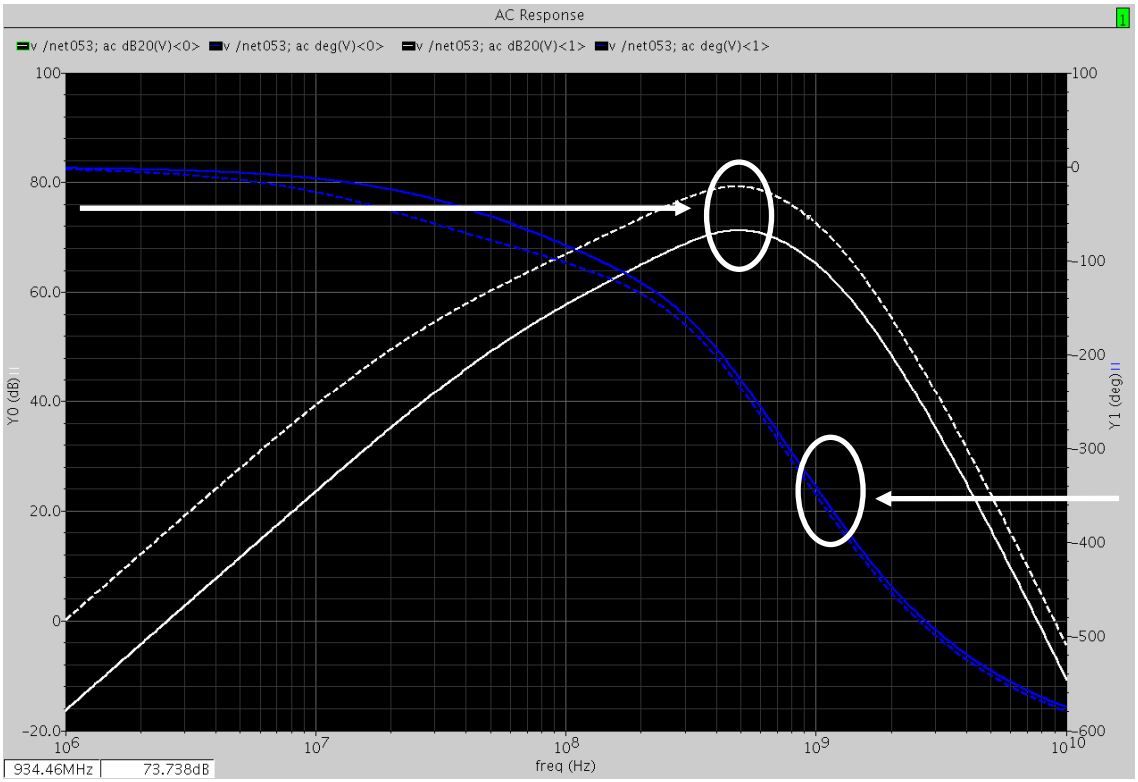


Fig. 4.20. AC gain and phase of the tunable TIA with active inductance cancellation

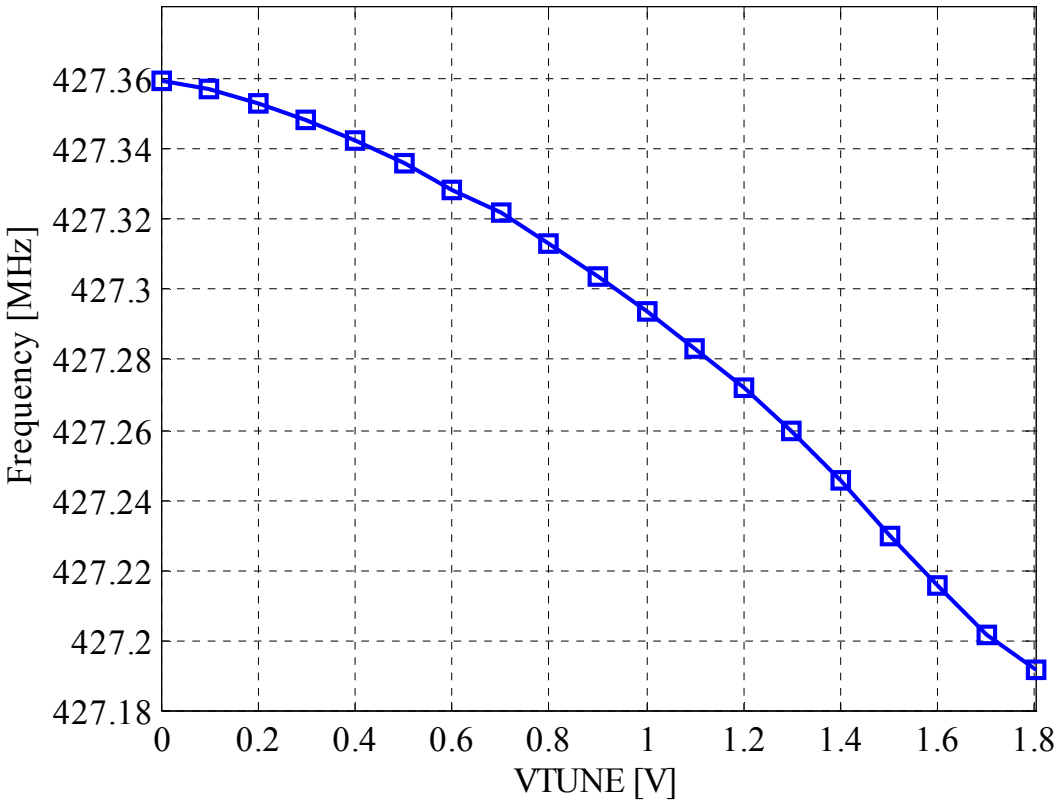


Fig. 4.21. Frequency vs. voltage for the 427MHz oscillator with active inductor

4.5.3 TIA with Negative Capacitance Cancellation

A three-stage feedback tunable TIA that uses negative capacitance for shunt parasitc cancellation is designed and fabricated in 0.18μm CMOS process. The core amplifier is the same as the one used for oscillator without tuning enhancement. Similarly, two series back-to-back varactors that are placed at the input of the TIA play the role of tuning network. The aforementioned single-port negative capacitance generation block is added to the input of the TIA for shunt parasitic cancellation. The load capacitance, C_L, is made tunable to allow for adjusting the negative capacitance value for best shunt parasitic cancellation result (Fig. 4.22).

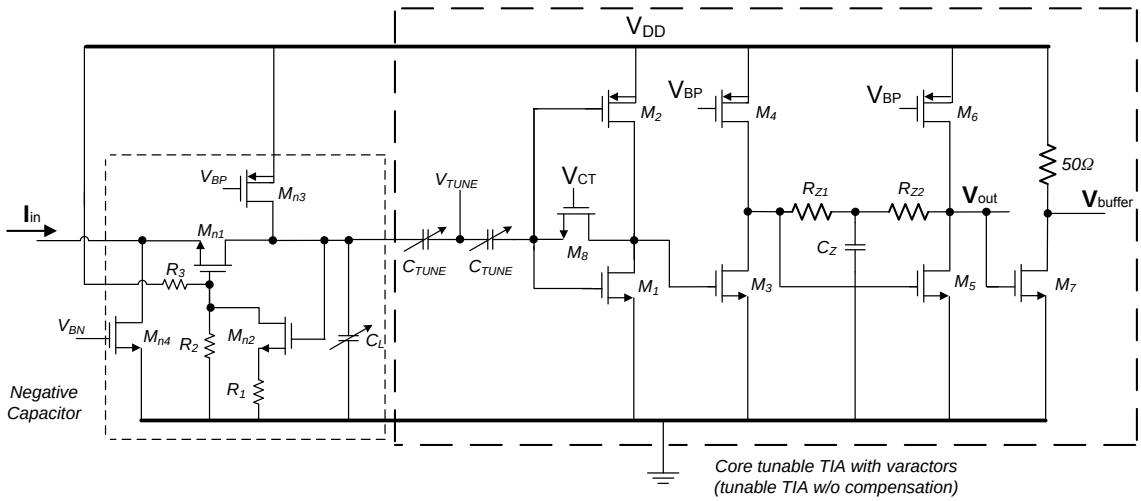


Fig. 4.22. Schematic of the tunable TIA with negative capacitor

The TIA (with temperature compensation) measures 1300μm×425μm (Fig. 4.23), consumes around 11.4mW, and is capable of providing gain > 72dBΩ up to 1.2GHz with 2pF input/output load. The gain can be tuned by ~12dB at the expense of smaller BW. Although, the impact of the tuning network on the transimpedance gain is reduced due to partial shunt parasitic cancellation but it is still considerable (>14dB) and can not be ignored. In this case, the transimpedance gain drops from 85dBΩ to around 72dBΩ when the tuning capacitance is varied from its maximum to the minimum (Fig. 4.24).

The TIA is interfaced with the same 427MHz AlN-on-Si lateral micromechanical resonator. The measured tuning range of the 427MHz micromechanical oscillator is beyond 810ppm (Fig. 4.25). The tuning range is ~2.3× larger than the oscillator with active inductance cancellation and more than 12× larger than the oscillator without shunt parasitic cancellation. This tuning range is now beginning to approach 1000ppm threshold that is necessary for fully-electronic temperature and/or process compensation in silicon micromechanical oscillators.

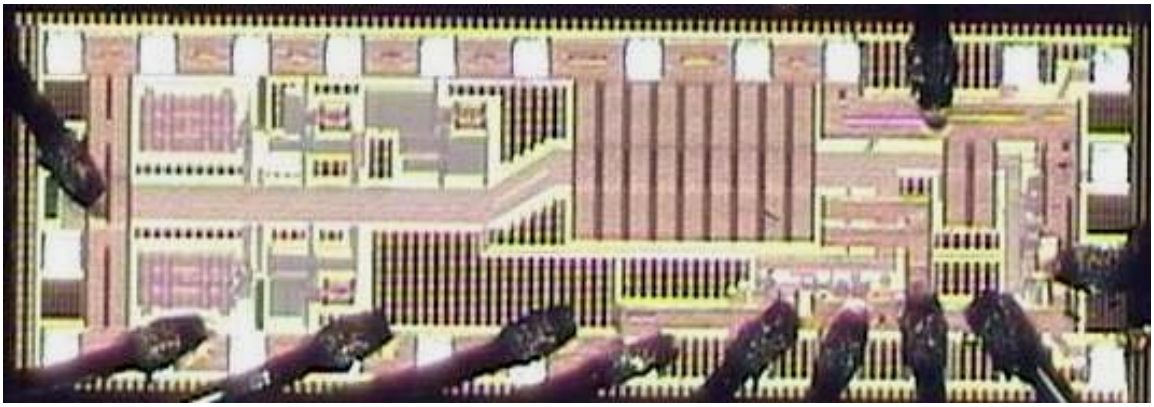


Fig. 4.23. Chip view of the TIA (and temp. compensation) with negative capacitor

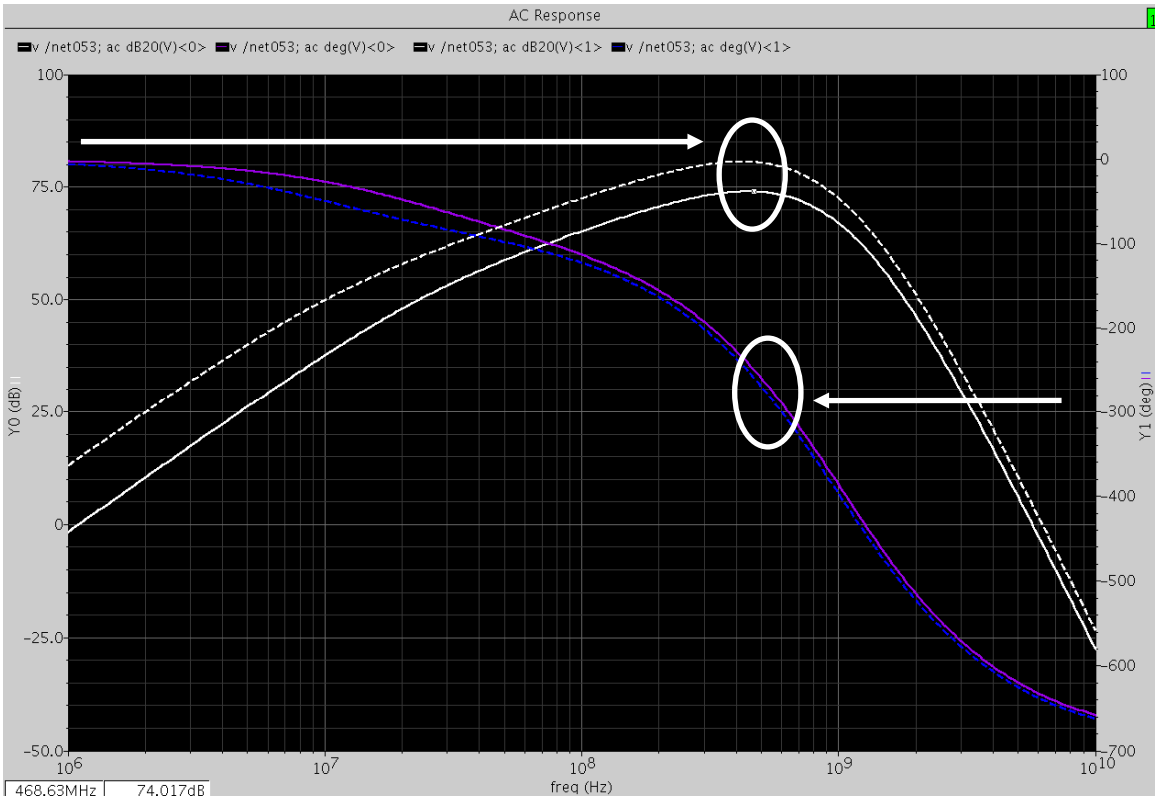


Fig. 4.24. AC gain and phase of the tunable TIA with negative capacitor

The measured phase-noise of the 427MHz oscillator across the tuning range is shown in Fig. 4.26. The phase-noise performance is better than -82dBc/Hz at 1kHz offset and floor reaches below -147dBc/Hz for the best case. The worse case phase-noise performance across the tuning range is also shown in Fig. 4.26. The tuning range is reduced when the

close-to-carrier (<10kHz) phase-noise degradation across the tuning range is kept within the 5dB mark of the best measured phase-noise profile. The phase-noise is slightly worse than the oscillators with active inductance cancellation and without tuning enhancement due to the higher noise associated with the negative capacitance generation circuitry. With proper sizing of critical transistors, it is possible to reduce the flicker noise contribution of this block that has a direct impact on the close-to-carrier phase-noise performance of the oscillator.

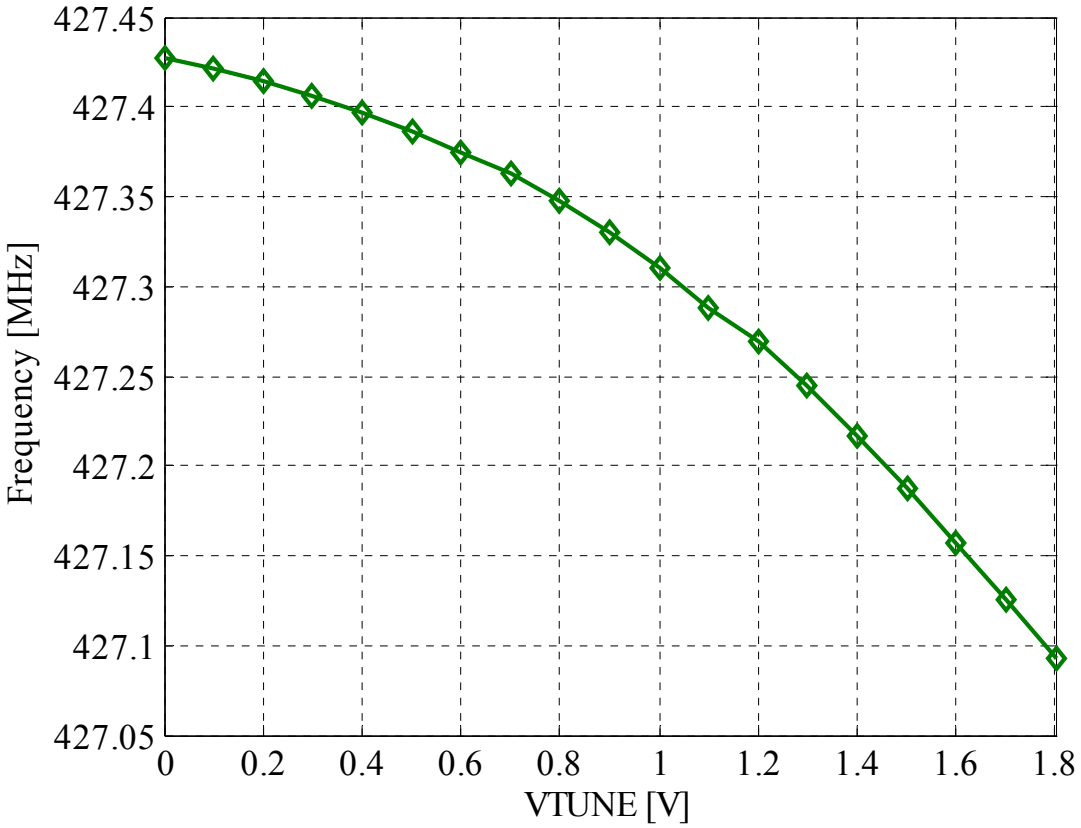


Fig. 4.25. Frequency vs. voltage for the 427MHz oscillator with negative capacitor

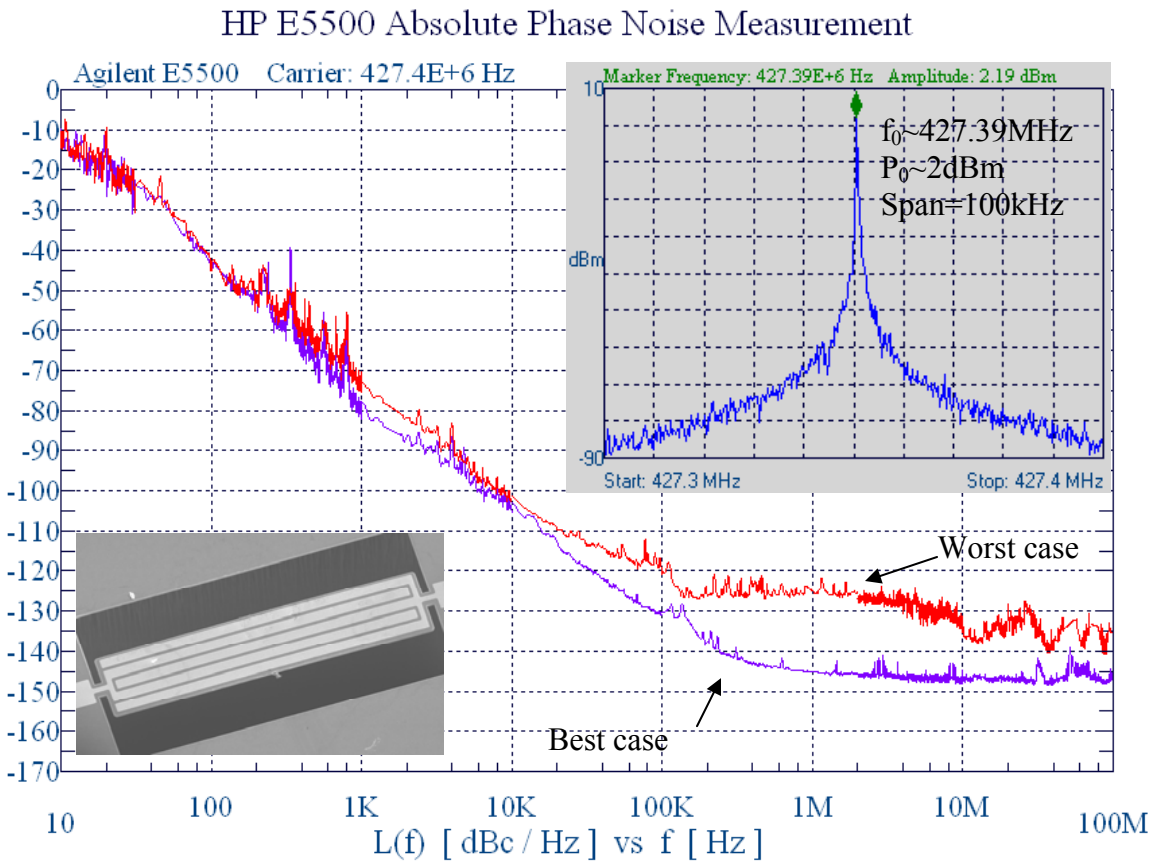


Fig. 4.26. Phase-noise of the 427MHz oscillator with negative capacitor

4.5.4 Comparison of Tuning Enhancement Techniques

Comparison of these techniques based on the maximum tuning range achieved with 427MHz oscillator is fairly straightforward; the TIA with negative capacitance achieves maximum tuning range beyond 810ppm that is 2.3× of that of the TIA with active inductor (~350ppm) and more than 12× of the 64ppm tuning achieved in a TIA without tuning enhancement (Fig. 4.27). However, the phase-noise performance gets affected when a shunt parasitic cancellation network is added. The close-to-carrier phase-noise degradation is below 4dB for the worst case, i.e. oscillator with negative capacitance cancellation. As such, the negative capacitance cancellation can be considered a viable technique to improve the tuning range with minimal phase-noise degradation.

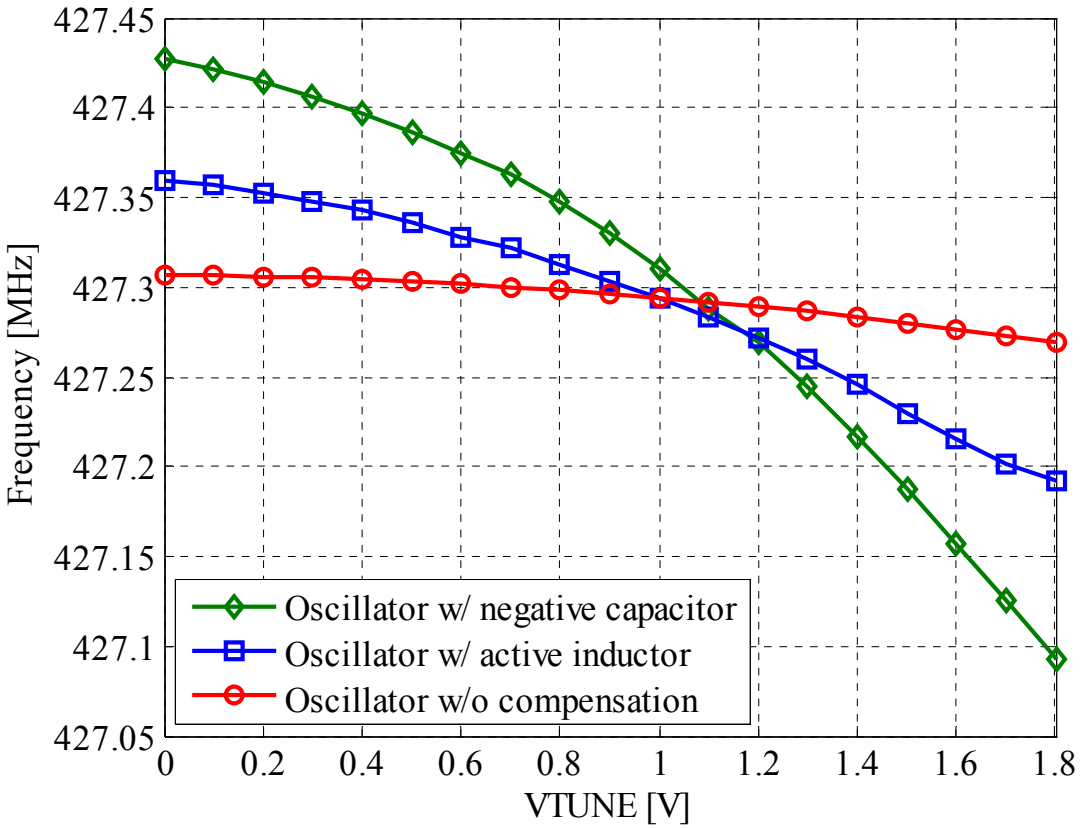


Fig. 4.27. Frequency vs. the tune voltage for 427MHz oscillators

4.6 Conclusion

In this chapter, different frequency tuning methods for micromechanical oscillators are studied. The chapter covered both the resonator-based and the electronic tuning techniques with emphasis on electronic tuning for lateral micromechanical oscillators. Two popular methods for frequency tuning, i.e. parallel and series tuning are discussed and their performance in lateral micromechanical oscillators are compared. The shortcoming of series tuning for lateral micromechanical oscillators with large shunt parasitic capacitance are identified and supported with detailed theoretical analysis of series tuning in such oscillators. Finally, tuning enhancement methods based on shunt

parasitic capacitance cancellations are introduced and supported with measured data from case studies to demonstrate the viability of each approach for high-frequency lateral micromechanical oscillators.

CHAPTER 5: Temperature Compensation for MEMS Oscillators

Frequency reference oscillators require very-high short-term and long-term accuracy to meet the requirement for modern radio transceivers. While the short-term accuracy can be addressed by reducing the phase-noise/jitter and suppressing the unwanted harmonics, the long-term accuracy calls for a comprehensive temperature compensation solution [1]. There are two major approaches for temperature compensation in micromechanical oscillators material-based [30], [44], [75] and electronic [22], [6] temperature compensation.

This chapter explores material and electronic temperature compensation techniques for lateral micromechanical oscillators. The chapter starts with introduction of material and electronic temperature compensation; the two most widely used approaches for temperature compensation. Then, it builds up on this foundation by introducing the open-loop electronic temperature compensation approach that can be adapted to a combination of these approaches. After that, it first goes into the system-level and then circuit-level implementation of open-loop electronic temperature compensation. The last portion of this chapter is dedicated to examples of micromechanical oscillators that benefit from material and electronic temperature compensation.

5.1 Introduction

Temperature compensation is the key to improve the long-term stability of reference oscillators. Material and electronic compensation are the two main candidates for lateral micromechanical oscillators. Material compensation involves the use of a material in the resonator design with opposite behavior with temperature. This approach is inherently

low power but it comes at the expense of Q reduction that is certainly not welcome for most low phase-noise applications. Electronic compensation, does not affect the resonator performance but it requires extra power beyond the sustaining amplifier and require accurate temperature sensors. In fact, the accuracy of the temperature compensation circuit is no better than that of the temperature sensors used in the compensation block.

Another complicating factor is the large drift (|TCF|>25ppm/ºC for silicon) of the high-Q micromechanical oscillators. This large TCF may prevent the micromechanical oscillator from achieving the stated total drift over a wide temperature range using only one of these compensation methods. As such, combination of material and electronic compensation may become necessary. The goal of this study is first to explore the limitation of both material and electronic compensation schemes to contain the total drift to less than ±50ppm across the industrial temperature range of -40ºC to 85ºC, and then propose alternative to deliver such accuracy.

5.2 Temperature Compensation Methods for Micromechanical Oscillators

Material and electronic temperature compensation methods are widely used in lateral micromechanical oscillators. The accuracy and impact of each method should be independently studied to determine its viability for high frequency micromechanical oscillator applications.

5.2.1 Material Compensation

In this approach, the frequency drift is compensated for by including a material in the micromechanical resonator structure that exhibit an opposite frequency vs. temperature behavior than the rest of the materials used in the resonator stack. Usually, the resonator

is made of materials with large negative TCF such as silicon and AlN. Hence, the compensation material should exhibit positive TCF. A famous candidate is silicon dioxide (SiO_2) with TCF around 3× larger (~80ppm/ºC) [30] than that of the silicon. A Carefully engineered silicon oxide to silicon ratio ensures near-zero TCF across a wide temperature range. The silicon oxide layer is embedded in the resonator stack (Fig. 5.1).

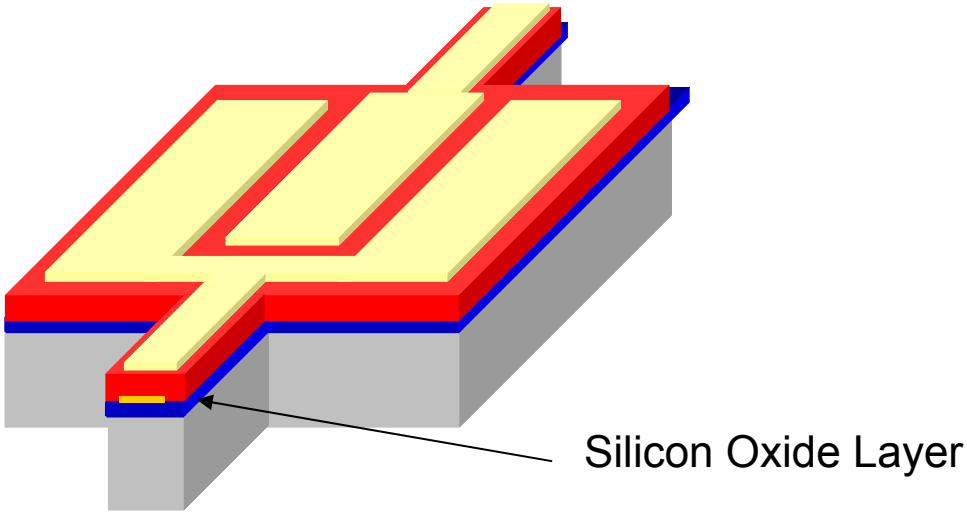


Fig. 5.1. Resonator structure with embedded silicon oxide layer for TCF reduction

The main disadvantage of this temperature compensation method is that most materials with large positive TCF exhibit significantly higher acoustic loss properties than the single-crystal silicon. This extra loss results in lower Q that is undesirable for low phase-noise reference oscillator applications [30]. One solution is to use another low acoustic loss material with inherently lower TCF such as Nanocrystalline Diamond (NCD) in the resonator structure to reduce the thickness of silicon oxide film [48]. Another important advantage of NCD film is the Q improvement due to inherently higher f.Q product [76].

5.2.2 Electronic Compensation

There are two major methods for electronic temperature compensation: closed-loop and open-loop methods. In closed-loop method, the designers rely on the output of the PLL to

compensate for frequency drift with temperature. This can be done either by an analog charge-pump PLL that uses a very accurate temperature sensing unit and a phase-frequency detector with known (and minimally varying) characteristic across the temperature range or through a fractional-N frequency synthesizer whose output frequency is determined with the help of a look-up table. The closed-loop approach is more accurate but at the same time, consumes more power. In an open-loop system, the compensation is achieved through accurate sensing of the temperature variation and using this information to generate a signal that is applied to the temperature compensation circuitry. Although a closed-loop system is potentially more accurate, it is complicated, requires large IC area and consumes large power. On the other hand, using an open-loop system with a very accurate temperature sensing unit and a custom analog function generator that can be used to accurately model the frequency drift of the oscillator with variation in temperature can provide up to 100× improvement over uncompensated across -40ºC to 85ºC temperature range [6]. The accuracy can be further improved to ±5ppm (that is comparable to TCXO's) with a more accurate electronic and/or combination of electronic and material compensation techniques.

Open-loop electronic temperature compensation takes advantage of electronic [47] and/or resonator-based [6] frequency tuning to accurately adjust the oscillation frequency in the presence of large variation in the environment temperature. The electronic temperature compensation block is comprised of three sub-units with tight accuracy specs: temperature sensing unit, control signal generation unit, and frequency tuning unit. The last block is usually embedded in the sustaining amplifier and is extensively covered in

chapter 4 of this dissertation. The temperature sensors are usually in the form of bandgap and proportional-to-absolute-temperature (PTAT) circuits. The design of control signal generation unit is dependent on the frequency vs. temperature behavior of the oscillator as well as the frequency tuning profile and can be more complicated [6]. Fig. 5.2 shows an example of electronic temperature compensation block used for 103MHz SiBAR oscillator [6].

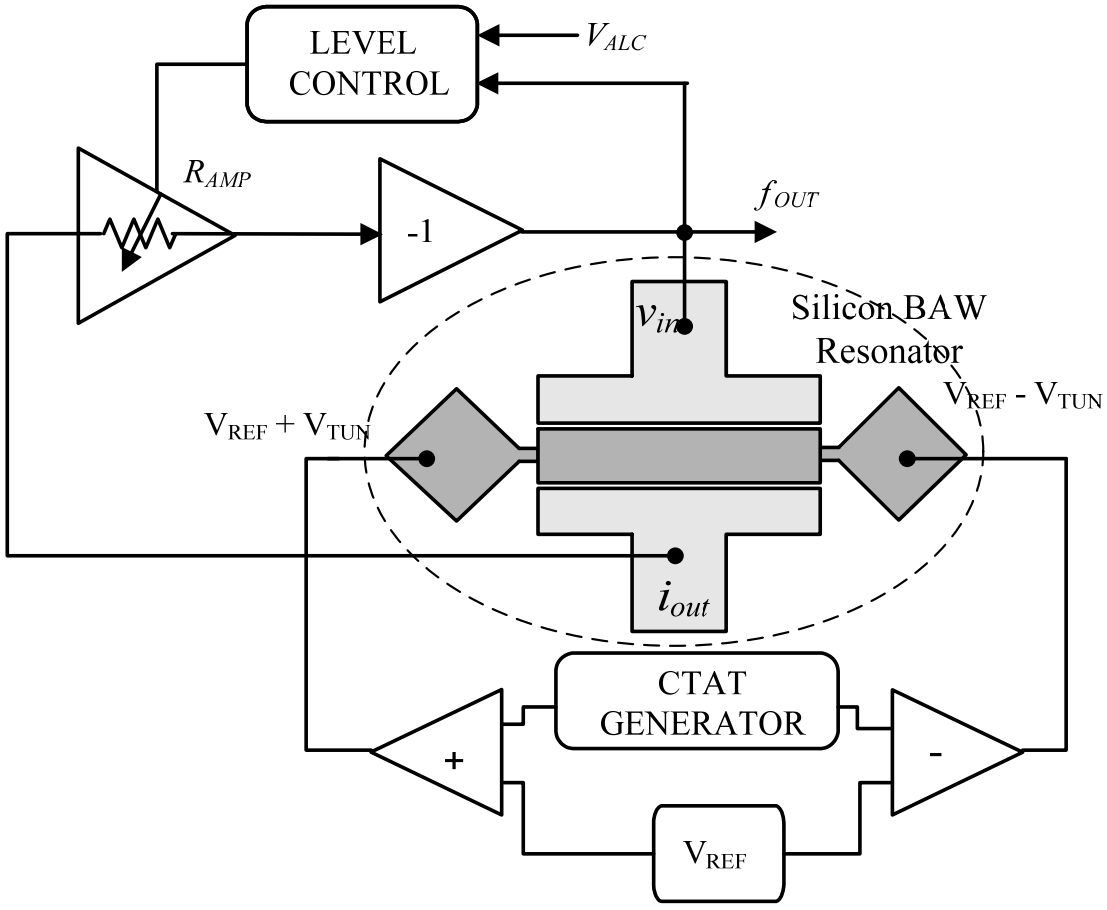


Fig. 5.2. Block diagram of temperature-compensated SiBAR oscillator [6]

The main disadvantages of the open-loop electronic compensation technique are the tight accuracy requirements for each of these three sub-blocks and the power consumption. While the power consumption can be lowered with a careful design [77], the only reliable

method to mitigate the accuracy concern is to use a closed-loop PLL-based electronic temperature compensation approach [78].

5.3 Implementation of Open-Loop Electronic Temperature Compensation

To better perform the design and optimization required for accurate open-loop electronic temperature compensation blocks, it is vital to have a system-level understanding of the block before moving to the detailed circuit-level implementation of each sub-block.

5.3.1 System-Level Implementation

A general block diagram for the open-loop temperature compensation bock is shown in Fig. 5.3. The frequency tuning unit is embedded with the TIA and is not shown here.

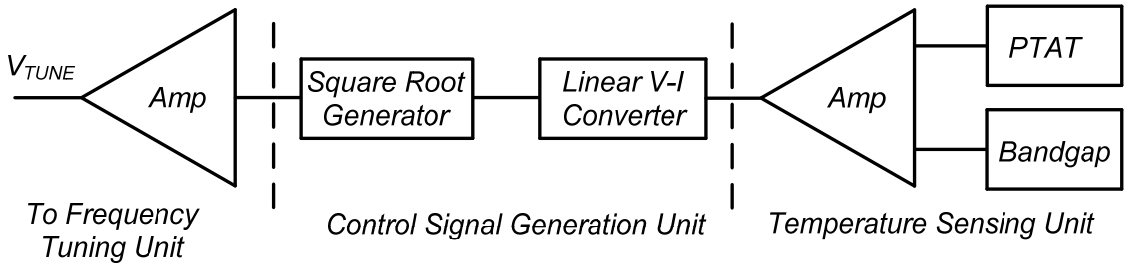


Fig. 5.3. Block diagram of the open-loop electronic temperature compensation

The temperature sensing unit includes the bandgap and PTAT temperature sensors. The temperature-insensitive output voltage of the bandgap reference is compared against the output of the PTAT circuit that linearly changes with temperature. The PTAT is used to generate an output signal (voltage or current) whose magnitude changes linearly with variation in absolute temperature. The comparison and scaling are done with a low-offset difference amplifier with appropriate resistive feedback network.

The design of control signal generation unit is dependent on the frequency vs. temperature drift of the oscillator. Usually the frequency vs. temperature behavior for

micromechanical oscillators can be approximated with a linear function, however, the frequency variation vs. tuning voltage for most tunable micromechanical oscillators is nonlinear. The resonator-based tuning techniques such as the electrostatic tuning rely on the change in the polarization voltage, V_p, of the resonator to induce frequency shift. Since the resonance frequency is proportional with V_p^2, the frequency vs. tuning voltage is nonlinear. For electronic tuning, the variation in the effective capacitance of the varactor with the tune voltage is a function of $(V_{tune})^{-n}$. This property combined with the nonlinear relationship between the oscillation frequency and varactor capacitance, i.e. $1/\sqrt{C_{tune}}$, makes the linear approximation obsolete.

To have a proper approximation of these two curves, it is necessary to express these function in Taylor series. For applications with moderate accuracy ($<\pm$50ppm), considering the first two terms (first and second-order terms) is sufficient. For this reason, an analog parabolic function generator is considered. To convert the signal back to linear domain, the inverse of this function, i.e. square root generator [79] must be included in the control signal generation unit. Since the input to the square root generator is current and the output of the temperature sensing unit is a voltage, linear V-to-I conversion for DC signals is necessary [47]. This can be done either by a transconductance amplifier [22] or by a linear V-to-I converter. A linear trannsconductance amplifier whose output is proportional to the g_m of the transistors will be prone to gain error due to the variation in process and temperature. This error combined with the inherent offset of the amplifier may limit the performance of the temperature compensation block. A novel linear V-to-I converter such as the one shown

in [47], on the other hand, functions more smoothly, has larger dynamic range and exhibits less non-idealities.

The output of the control signal generation unit is then scaled and fed to the tuning network to adjust the oscillation frequency. The frequency control unit is either part of the sustaining amplifier (for electronic tuning) or provides a signal to the resonator for frequency tuning.

5.3.2 Circuit-Level Implementation

The temperature sensing unit consists of three sub-blocks: bandgap, PTAT, and difference amplifier. The bandgap reference is based on a V_{BE}-ΔV_{BE} architecture with extra cascade devices and error amplifier to reduce the bandgap curvature [22] (Fig. 5.4). Similar topology with different resistance ratio is used to realize the PTAT reference (Fig. 5.4). Both circuits are optimized for the best performance from -40ºC to 85ºC. The simulated and measured outputs of the bandgap and PTAT references are in good agreement (Fig. 5.5 and 5.6). The PTAT slope is around 1.7mV/ºC. The temperature coefficient of the bandgap cell is around 27ppm/ºC.

The difference amplifier is a simple two-stage differential-input single-ended output operational transconductance amplifier (OTA) with miller compensation. The overdrive voltages on input MOS transistors are maximized to reduce the input offset due to the mismatch in the transistors (Fig. 5.7).

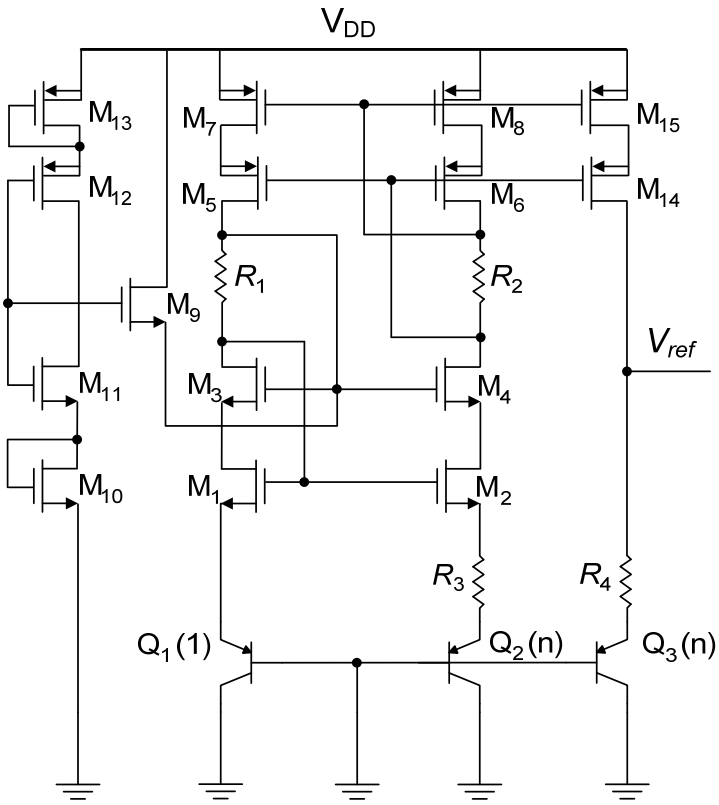


Fig. 5.4. Schematic of the bandgap and PTAT reference generators

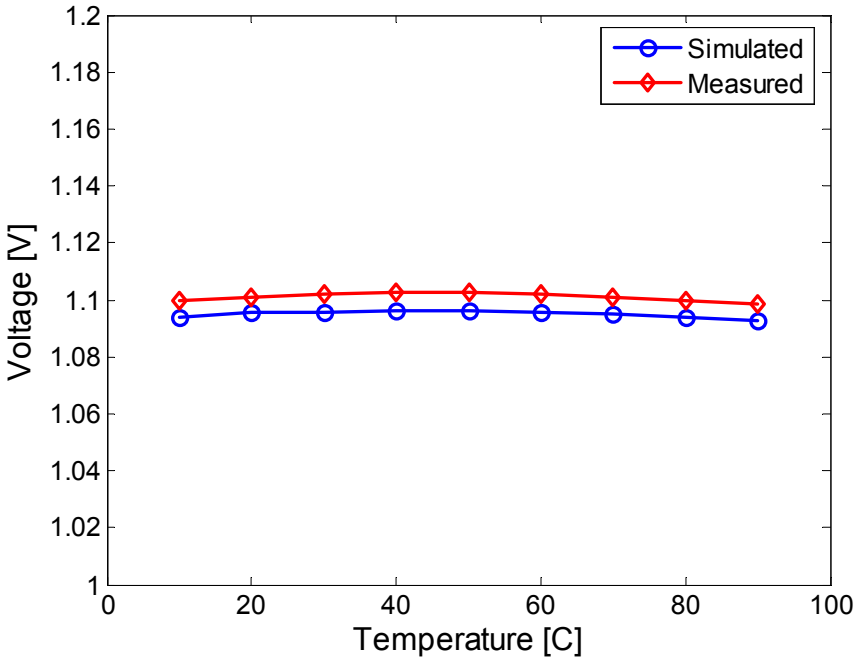


Fig. 5.5. Simulated and measured output of the bandgap reference

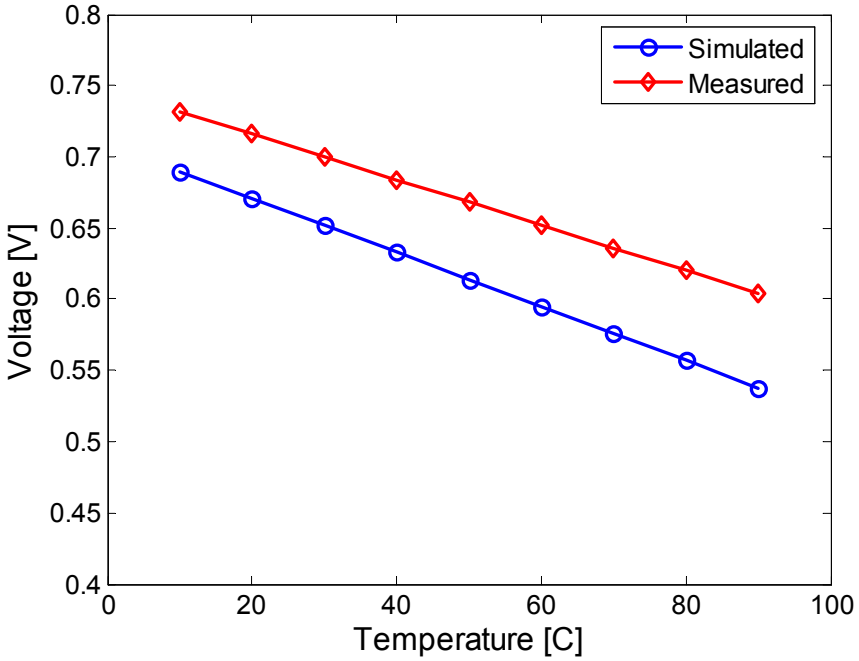


Fig. 5.6. Simulated and measured output of the PTAT reference

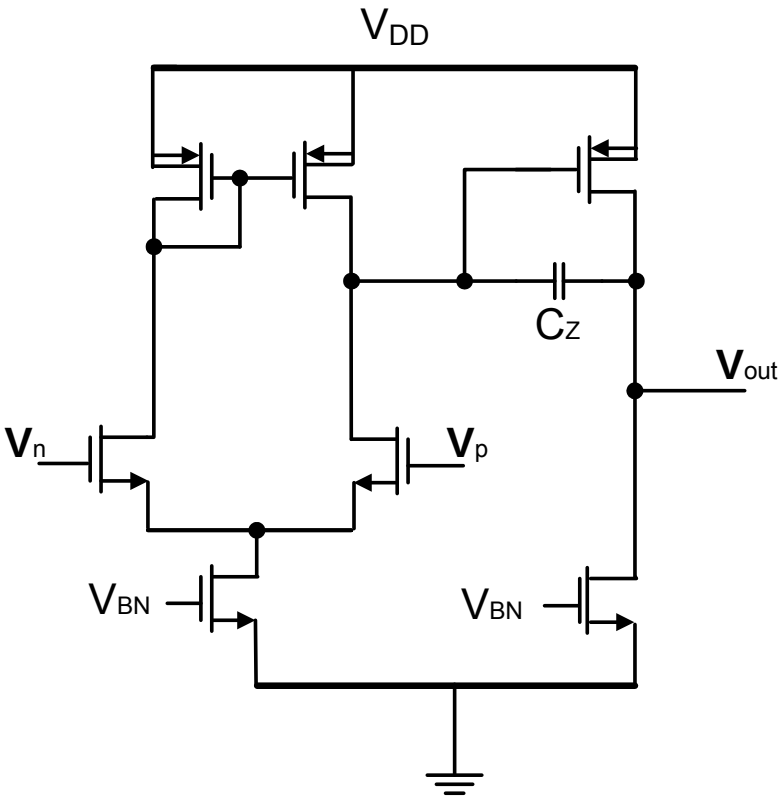


Fig. 5.7. Schematic of the two-stage OTA with miller compensation

The square-root generator uses an amplifier in shunt feedback configuration whose input is connected to the source of a diode-connected device that passed the reference current. The output voltage of the circuit is proportional to the square-root of the reference current reference current that passes through M_1 (Fig. 5.8). The detailed design of square-root generator is given in [79] and won't be repeated here.

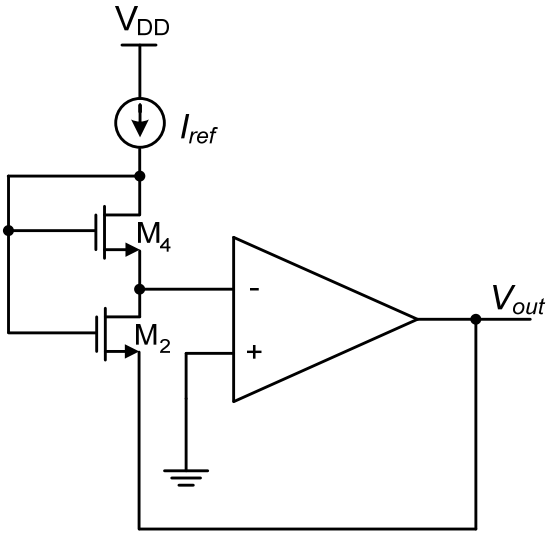


Fig. 5.8. Block diagram of the square-root generator [22]

The design of linear V-to-I converter is critical since its performance is directly related to the accuracy of the square-root generator. The schematic of the linear I-to-V converter is shown in Fig. 5.9. Neglecting the channel-length modulation effect in M_1 transistor, the current that passes through M_1 and M_2 is proportional to square of V_{in}. This current forces a certain V_{GS} across the M_2 device which is proportional to the square root of this current and consequently, linearly dependent to the input voltage. Therefore, the output current, I_{out}, generated by dropping this voltage across the resistor is linearly proportional to the input voltage, V_{in}. The input to output relationship can be approximated by:

$$I_{out} \approx \frac{1}{R_2}.\left[V_{TH,M1} + \sqrt{\frac{K_n\left(\frac{W}{L}\right)_{M1}}{K_p\left(\frac{W}{L}\right)_{M2}}}.\left(V_{in} - V_{TH,M2}\right)\right], \tag{5.1}$$

where $V_{TH,M1}$ and $V_{TH,M2}$ are the threshold voltages of M_1 and M_2 devices, respectively. The output of the linear V-to-I converter is shown in Fig. 5.10. The deviation from linear line is very small demonstrating the high accuracy of this block. The main source of error in this block is the channel-length modulation effect. This error can be reduced by proper sizing of M_1 and M_2 transistors. Finally, the output of the square-root generator when connected to the linear V-to-I converter is shown in Fig. 5.11. The sources of error in this block include the nonlinearity due to the body effect of M_1 transistor and gain error in the amplifier both of which can be suppressed by design optimization.

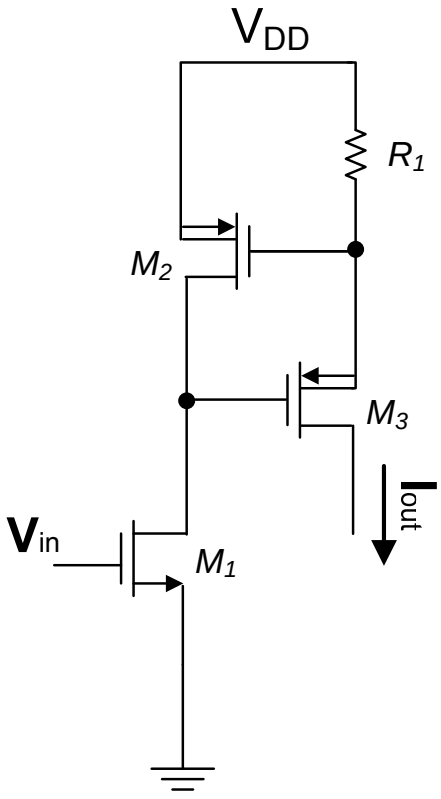


Fig. 5.9. Schematic of the linear V-to-I converter

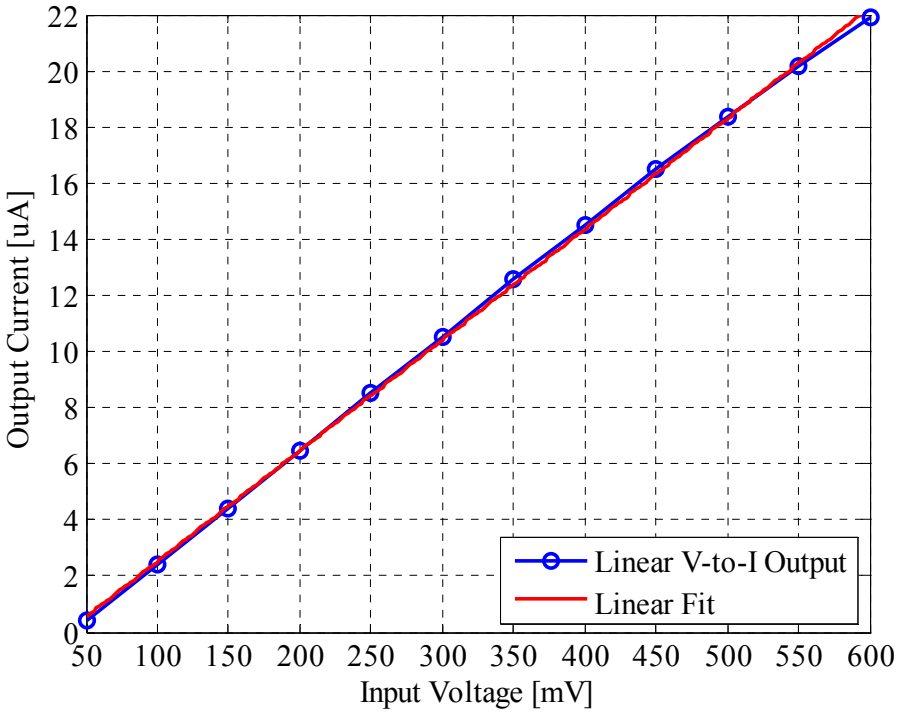


Fig. 5.10. Output current of the linear V-to-I converter

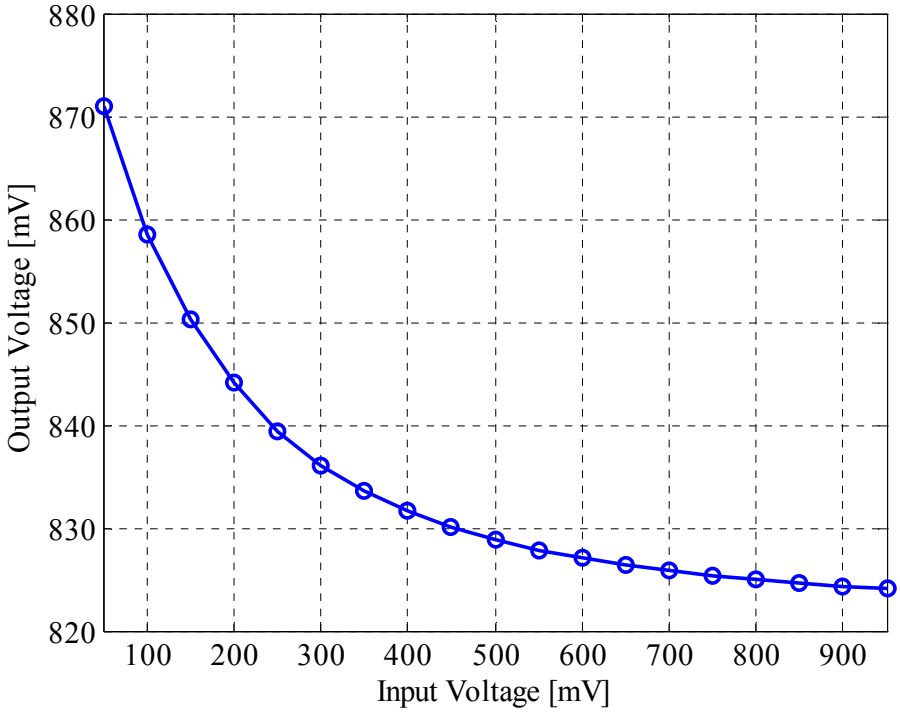


Fig. 5.11. Output of the square root generator and linear V-to-I converter

5.3.3 Sources of Error

There are four major sources of error:

- Bandgap and PTAT non-idealities: Usually appear as bandgap and PTAT curvature.
- Amplifier offset: Inaccuracy of difference and scaling operations
- Square-root generator error: Error in approximating a parabolic response
- Linear V-to-I converter error: Indirectly affect the parabolic response approximation

Among these four error sources, the last two are more important and should be minimized by careful optimization for high performance applications. The bandgap and PTAT errors can be easily reduced by using low-curvature circuits.

5.4 Case Studies

In this section, two temperature-compensated high-frequency lateral micromechanical oscillators are presented: the first oscillator uses a 441MHz AlN-on-Si resonator whose TCF brought near-zero by a thin silicon oxide film (material compensation); the second oscillator is based on a low-TCF 427MHz resonator with electronic temperature compensation.

5.4.1 Temperature-Compensated 441MHz AlN-on-Si Oscillator

A 0.18μm three-stage feedback tunable TIA similar to the one reported in [7] is interfaced with a 441MHz temperature-compensated AlN-on-Si micromechanical resonator. The resonator is fabricated on a ~1.5μm-thick CMOS-grade silicon substrate and uses a thin (~0.7μm) silicon oxide layer to reduce the TCF of the resonator to ~1ppm/ºC in -40ºC to 85ºC. Due to the use of lossy silicon oxide layer, the unloaded Q ($Q_{unloaded}$) of the resonator is degraded to ~1,100 with motional resistance close to 500Ω

(Fig. 5.12). In addition, the frequency is substantially shifted down due to the lower acoustic velocity in silicon oxide.

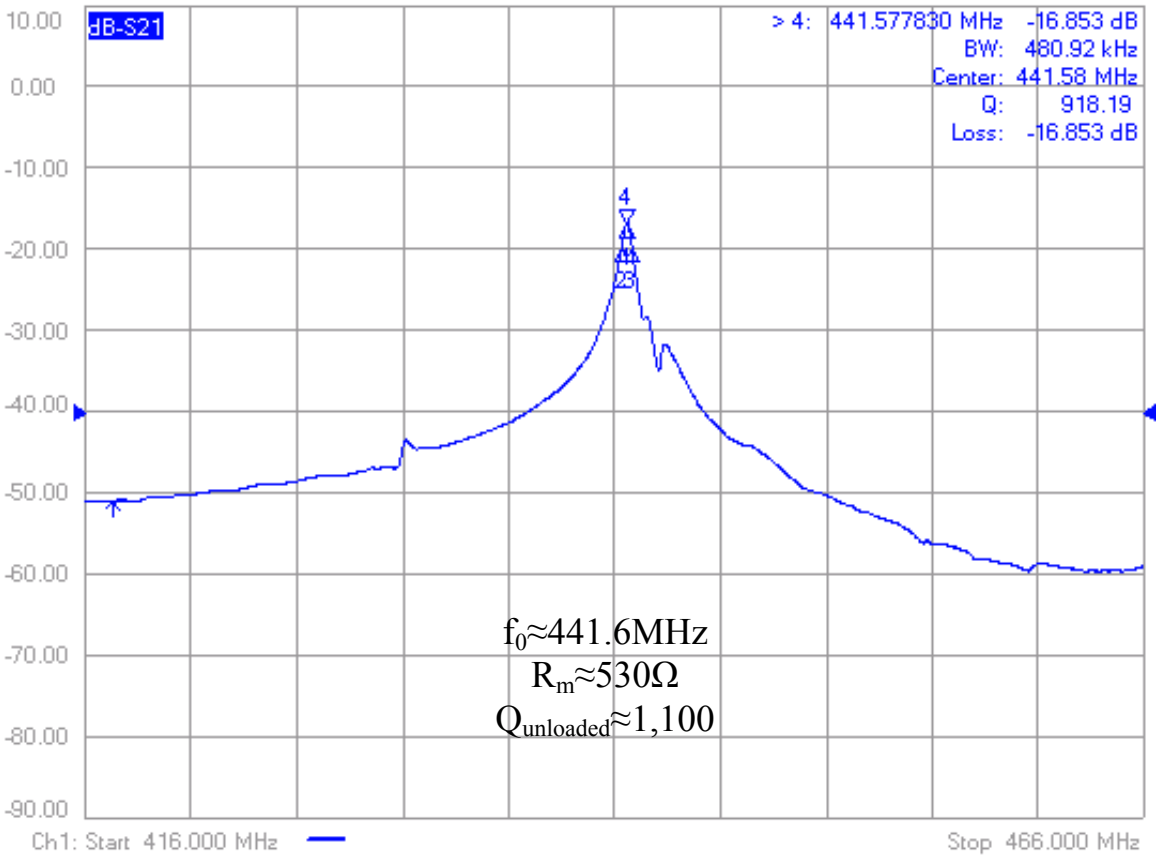


Fig. 5.12. Response of the temperature-compensated 441MHz AlN-on-Si resonator

The 441MHz AlN-on-Si micromechanical resonator is interfaced with the three-stage tunable TIA to sustain the oscillation. Then, the frequency drift of the oscillator across the -40ºC to 85ºC temperature range is measured under the vacuum. The operation under the vacuum eliminates the potential inaccuracies in the measurement due to the environments such as humidity. The results shows less than 140ppm total drift in -40ºC to 85ºC temperature range that is only 2× more than uncompensated quartz crystal oscillators (Fig. 5.13).

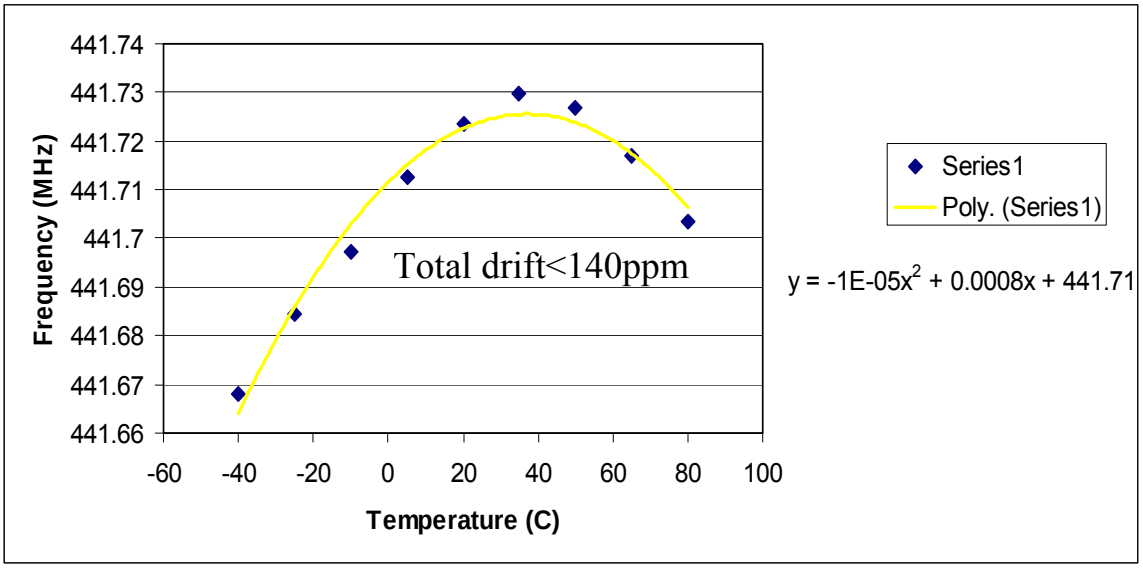


Fig. 5.13. Frequency drift of the 441MHz micromechanical oscillator

The measured phase-noise performance of the 441MHz AlN-on-Si micromechanical oscillator resonator is shown in Fig. 5.14. The close-to-carrier phase-noise is around -79dBc/Hz at 1kHz offset. The phase-noise floor reaches -152dBc/Hz. The close-to-carrier performance is affected by low Q of the resonator that is partly due to the use of silicon oxide in the resonator stack.

The close-to-carrier phase-noise degradation is the inherent problem for micromechanical reference oscillators that use material temperature compensation and remains the main obstacle toward their successful commercialization. This problem can be addressed by using materials with lower acoustic loss for compensation or placing the lossy silicon oxide layer as far away from the electrodes as possible. One way to realize such as resonator is to use the relatively-thin (<2μm) buried silicon oxide layer (BOX) available in most silicon-on-insulator (SOI) starting substrates [44]. Another problem is large spurs in far-from-carrier performance that is due to poor power handling of the

micromechanical resonator. This phenomenon can be partly explained by the low stiffness of the silicon oxide layer.

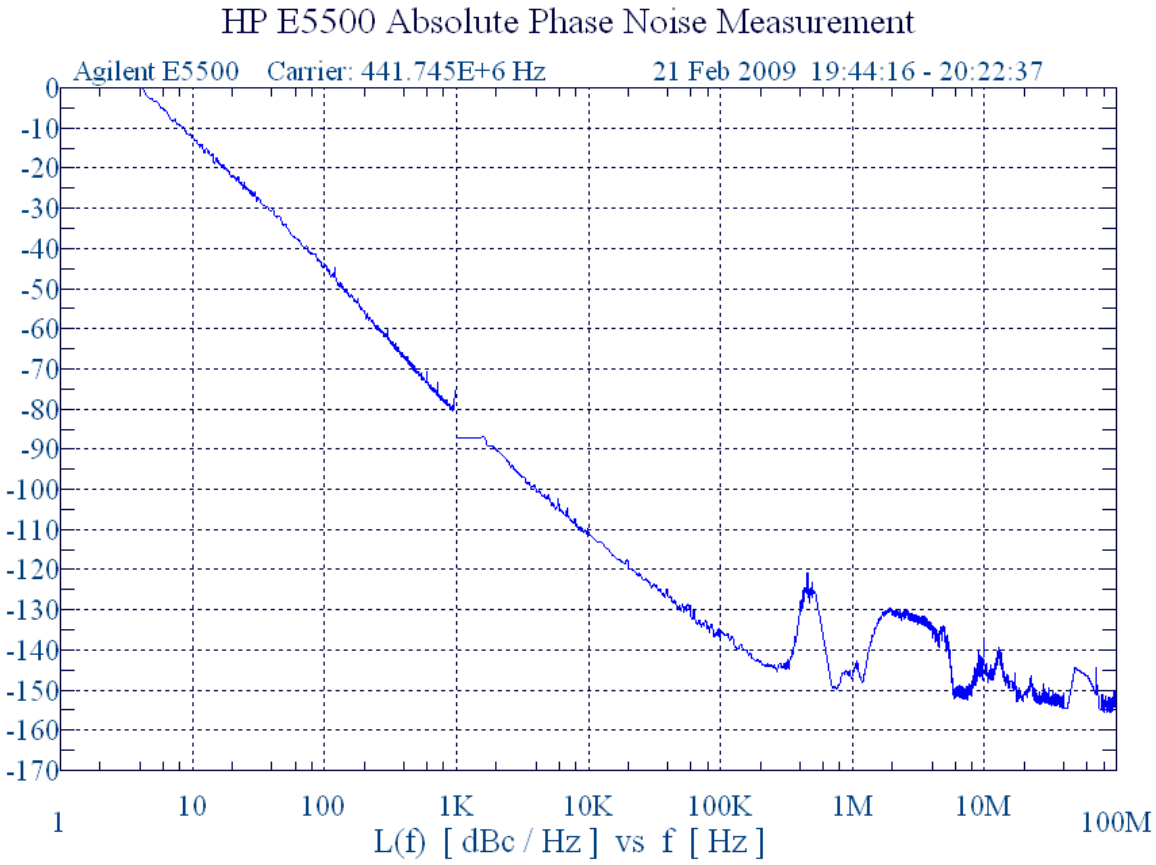


Fig. 5.14. Measured phase-noise of the 441MHz micromechanical oscillator

5.4.2 Electronically Temperature-Compensated 427MHz AlN-on-Si Oscillator

The 427MHz AlN-on-Si micromechanical resonator uses a very thin silicon oxide layer to lower the native TCF of the resonator to -10ppm/ºC. Then an open-loop temperature compensation circuit is used in combination with a tunable oscillator to deliver a sub-ppm/ºC 427MHz micromechanical reference oscillator [47]. The design approach and characterization data of the sustaining amplifier, electronic frequency tuning network and negative capacitance cancellation circuit for tuning enhancement are readily provided in chapter 4 of this dissertation.

Fig. 5.15 shows the block diagram of the temperature-compensated oscillator. The fully on-chip 2mW temperature compensation circuit burns 2mW and includes bandgap and PTAT references for temperature sensing, low-offset amplifiers for difference and scaling, and square-root generation circuitry [79]. A linear DC voltage-to-current converter is also added for better accuracy. The frequency tuning and phase-noise results are reported in chapter 4. Moreover, the design and characterization data for the building blocks of the temperature compensation block are provided earlier in this chapter.

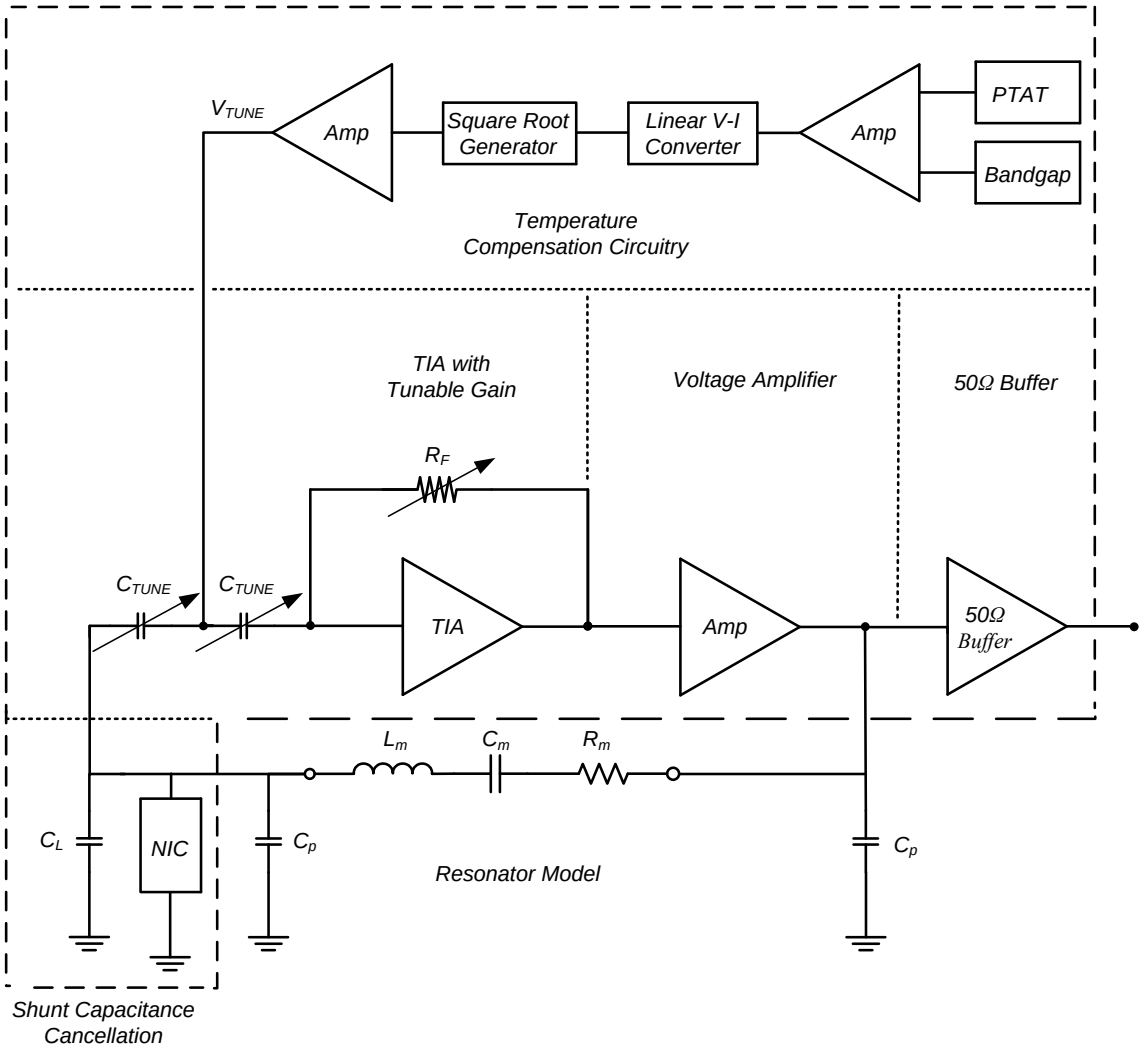


Fig. 5.15. Diagram of the electronically temperature-compensated oscillator

Using the open-loop electronic compensation technique, the temperature drift of the 427MHz oscillator is reduced from 780ppm to 70ppm in -10ºC to 70ºC range (Fig. 5.16). Removing the square-root generator and linear DC V-to-I converter increases the drift to more than 340ppm that shows the importance of this nonlinear compensation technique. This result shows over 34× improvement from the uncompensated oscillator and is comparable with a typical uncompensated quartz crystal oscillator.

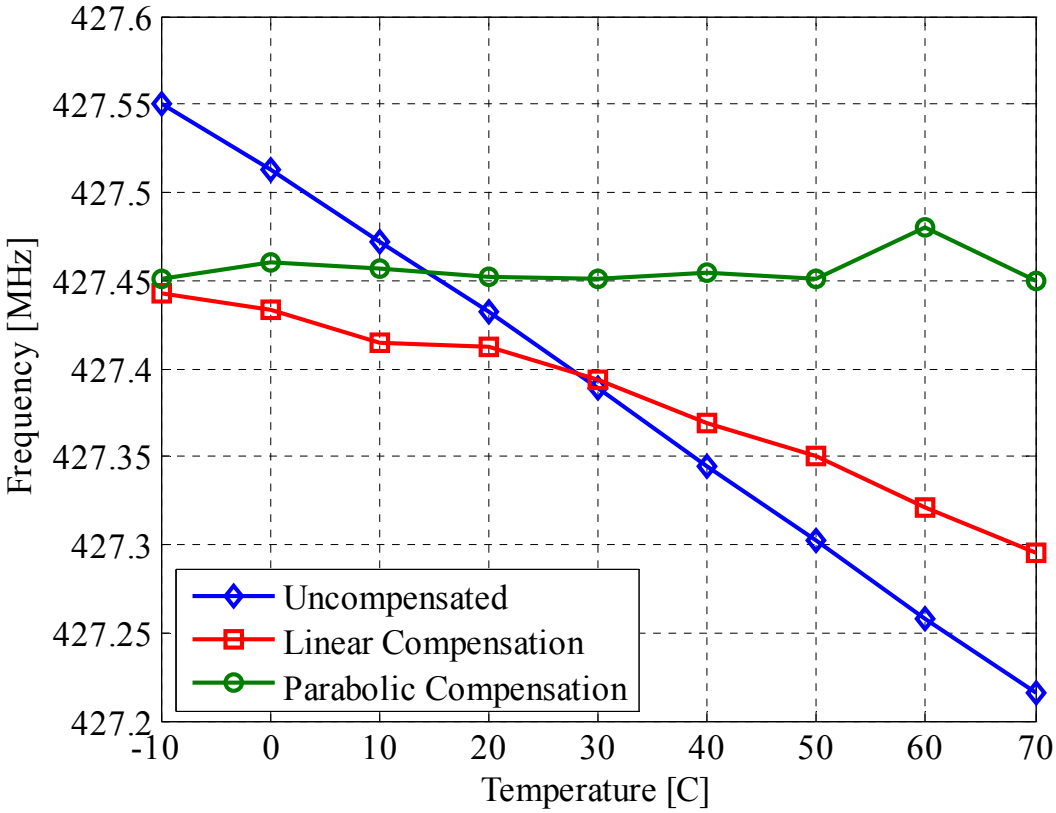


Fig. 5.16. Variation in oscillation frequency vs. temperature in -10ºC to 70ºC range

5.5 Conclusion

Temperature compensation is an integral part of any micromechanical reference oscillator. This section introduced, explained the design methodology, and provided

examples of, two major temperature compensation techniques for micromechanical oscillators: material and electronic temperature compensation. Material compensation is a low-power approach but it negatively affects the Q and power handling of the resonator, both of which detrimental for low phase-noise micromechanical oscillators. Electronic compensation, on the other hand, minimally affects the oscillator performance but it requires complicated electronics with potentially high power consumption.

CHAPTER 6: Phase-Noise in Series-RLC Lateral MEMS Oscillators

Lateral micromechanical oscillators are gaining currency as the frequency references for modern radio transceivers due to their higher frequency of operation, larger tuning, smaller from-factor and potential integration with IC [6], [47], [66]. However, the short-term stability of these oscillators, which is the single most important performance criterion in reference oscillators, remains inferior to conventional quartz crystal oscillators, even though theoretical studies [13], [80] suggest otherwise. Therefore, accurate prediction of short-term stability is necessary.

The short-term stability of a reference oscillator is typically expressed in the form of jitter or phase-noise [7]. Work pertaining to modeling the phase-noise of micromechanical oscillators has largely focused on fitting the classical linear models such as Leeson's [81] to the observed phase noise characteristic [82], [83]. While the classical phase noise theories [81], [84], which focus on an LTI approach, provide reasonable phase-noise estimates for crystal type oscillators, their track record in accurately predicting the phase-noise performance of series-resonant lateral micromechanical oscillators is not promising. Of particular importance are the so-called empirical parameters in the classical theory whose values significantly differ for oscillators that are share the same sustaining amplifier but use similar resonators (Q and loss) with different parasitic. This requires careful consideration of the resonator parasitic impedances on the phase-noise of the micromechanical oscillator.

This chapter deals with the study of phase-noise in series-resonant lateral micromechanical oscillators focusing on both capacitive and piezoelectric oscillators. First, several well-known phase-noise models are introduced and their advantages are discussed. Then, before diving into the details of analytical modeling, several sources of phase-noise in micromechanical oscillators are briefly mentioned. After that, the discussion continues with the application of classical Leeson's theory to micromechanical oscillators. The contribution of first- and second-order parasitics on the phase-noise performance of lateral micromechanical oscillators is studied. This leads to an analytical expression for phase-noise of high frequency lateral micromechanical oscillators in presence of the finite motional resistance, shunt parasitic, and amplifier loading. Finally, examples of high frequency capacitive and piezoelectric micromechanical oscillators are provided to validate the derived analytical model.

6.1 Introduction

Non-idealities in the oscillator whether from the frequency selective tank such as finite Q and loss or from amplifier such as electronic noise cause widening in the oscillation spectrum. The degree to which the oscillation power is speared across the frequency spectrum is determined by the phase-noise of the oscillator. The relative phase-noise is defined as the average power carried in 1 Hz of the oscillation spectrum when normalized to the carrier power, P_C (Fig. 6.1):

$$L(df) = 10\log\frac{P_{1Hz}|_{df}}{P_C}, \tag{6.1}$$

where the L(df) is the relative phase-noise and P_{1Hz} is the average power carried in 1Hz of the oscillation spectrum at the frequency "df" offset from the oscillation frequency.

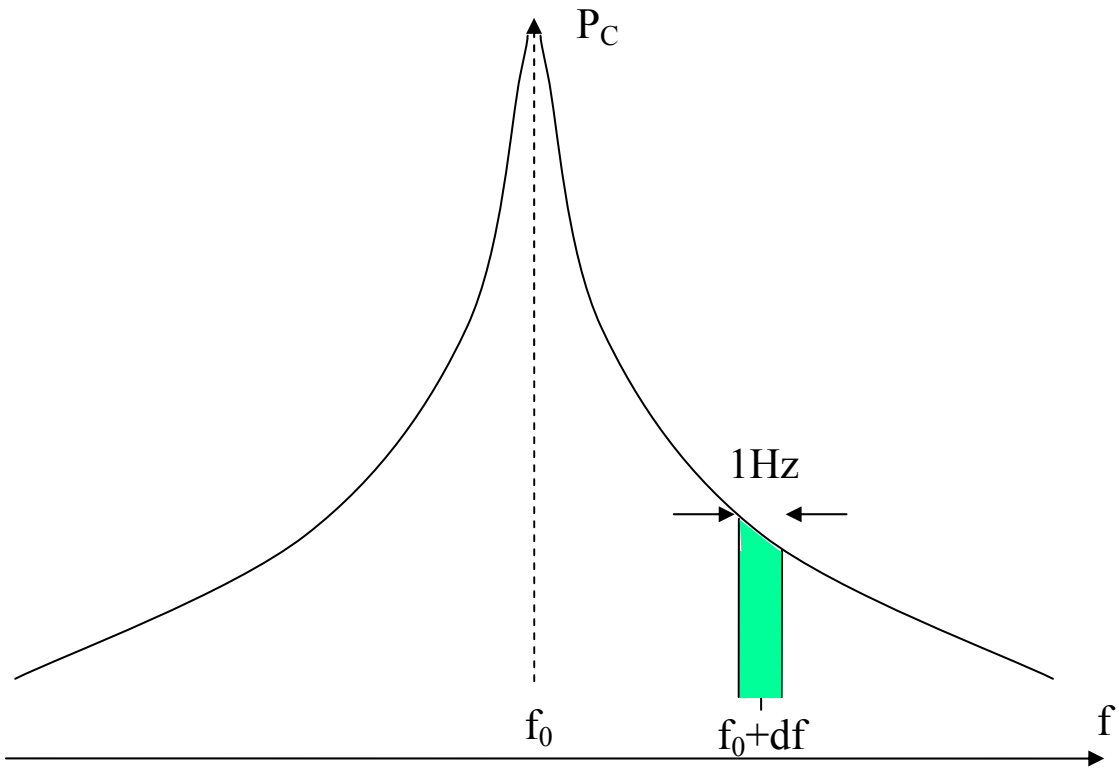


Fig. 6.1. Concept of phase-noise in oscillators

The phase-noise of an oscillator is another way of expressing its frequency fluctuations [84]. Stability measurements using frequency comparators give the spectral density of frequency fluctuations:

$$S_{\Delta f}(f_m) = \Delta f_{rms}^2, \tag{6.2}$$

where $S_{\Delta f}(f_m)$ is spectral density of the frequency fluctuations, Δf_{rms}. The phase-noise of the oscillator at the frequency "f_m" offset from the carrier frequency "f_0" is expressed by:

$$L(f_m) = \frac{S_{\Delta f}(f_m)}{2 f_m^2}. \tag{6.3}$$

The phase-noise is usually measured and expressed in decibels rather than absolute value:

$$L(f_m) = 10\log_{10}\left(\frac{\Delta f_{rms}}{\sqrt{2} f_m}\right)^2. \tag{6.4}$$

In a feedback oscillator, the mechanical and electronic noise (both thermal and flicker) are aliased around the oscillator frequency and are filtered by the frequency selective tank. This phenomenon creates an oscillator phase-noise profile with different regions. Fig. 6.2 shows the typical phase-noise spectrum of a feedback oscillator with common electronic (and possibly mechanical) noise sources [84]. There are 5 different regions with potentially different behavior. Some of these regions may be masked by others for oscillators with high-Q resonating tank.

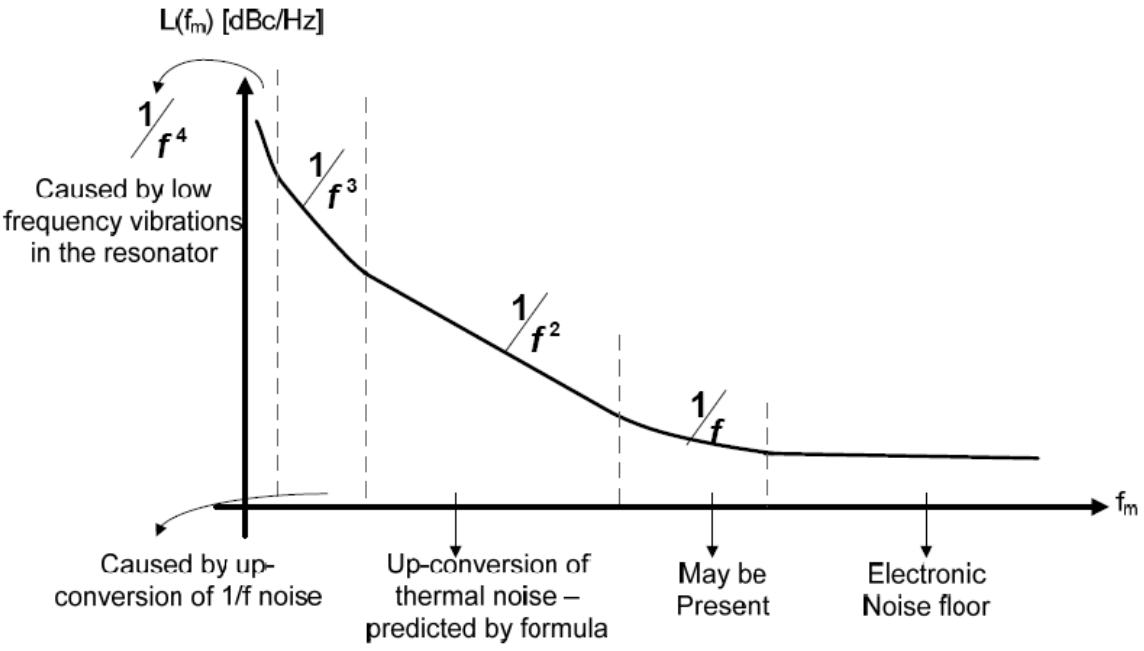


Fig. 6.2. Phase-noise spectrum of a typical feedback oscillator

The first region is the $1/f^4$ (f^{-4}) region which is referred to as random walk frequency modulation (FM). This region appears very close to the carrier and is typically due to the random variation in the frequency of the tank. For micromechanical oscillators, this phenomenon can be partly explained by the excessive low-frequency noise originating from the vibrating mechanical structure. Other contributing factors are resonator

nonlinearity (including the nonlinearity of the transducer and limited power handling capability), particle adsorption and desorption, and the Brownian noise [6], [83].

The $1/f^3$ (f^{-3}) region, called flicker FM, appears in close-to-carrier region and is the result of up-conversion of flicker noise (1/f noise) of the amplifier after it is aliased into the oscillation spectrum. For CMOS amplifiers with large flicker noise corner, the $1/f^3$ region extends well into several tens of kilohertz.

The $1/f^2$ (f^{-2}) region, called white FM or random walk phase, is due to the up-conversion of thermal noise (mostly from the amplifier) whose power spectral density (PSD) remains constant with frequency. For amplifiers with small flicker noise corner (such as bipolar amplifiers) or oscillators with low-Q tank (such as LC oscillators) this region is extended to from both ends into the close-to-carrier and far-from-carrier regions.

The 1/f (f^{-1}) region, called flicker phase, is transition region between the thermal noise and the noise floor of the oscillator. For oscillators that use high-Q tanks, the 1/f region is dominant and bridges the $1/f^3$ and noise floor regions. The noise floor, f^0 region, is limited by the noise of the electronics (including the buffer and other control circuits) that are used in the oscillator.

6.2 Analytical Models for Phase-Noise

Several models have been used by IC designers to predict the phase-noise performance of oscillators. These analytical models can be categorized into two general categories: linear and nonlinear models. This section briefly introduces these well-known models.

6.2.1 Classical Linear Time-Invariant (LTI) Model (Leeson's Model)

In the LTI approach, the noise generated from the amplifier (and possibly the resonator) is passed through the feedback loop. This noise (the amplitude and phase) is modulated to the carrier frequency. Assuming an amplifier with noise factor "F" and flicker noise corner "f_c", the PSD of the noise at frequency "f_m" offset from the carrier frequency is:

$$S_n(f_m) = kTF\left(1+\frac{f_c}{f_m}\right), \tag{6.5}$$

where k is the Boltzman's constant, T is the temperature in Kelvin. Assuming that half of this noise spectrum contributes to the phase noise and the other half to the amplitude, the phase-noise in dB can be expressed as:

$$L(f_m) = 10\log_{10}\frac{kTF}{2P_s}\left(1+\frac{f_c}{f_m}\right), \tag{6.6}$$

where P_s is the power of the carrier signal. For closed-loop systems with feedback factor other than unity, the phase-noise expression is more complicated. Feedback oscillators such as the one shown in Fig. 6.3 not only modulate the noise of each block but also filter the noise by passing it through the frequency selective tank with a very narrowband frequency response. The PSD of the output noise can be expressed by:

$$S_{\theta,out}(f_m) = S_{\theta,in}(f_m).\left|G_{noise}(f_m)\right|^2, \tag{6.7}$$

where $S_{\theta,in}(f_m)$, $S_{\theta,out}(f_m)$ are the PSD spectra of input and output phase-noise, respectively. $G_{noise}(f_m)$ is the closed-loop transfer function of the feedback system which depends on the frequency response of the resonating tank. Since the PSD of the input phase-noise is readily available from (6.6), the problem is reduced to finding the closed-loop transfer function of the feedback oscillator.

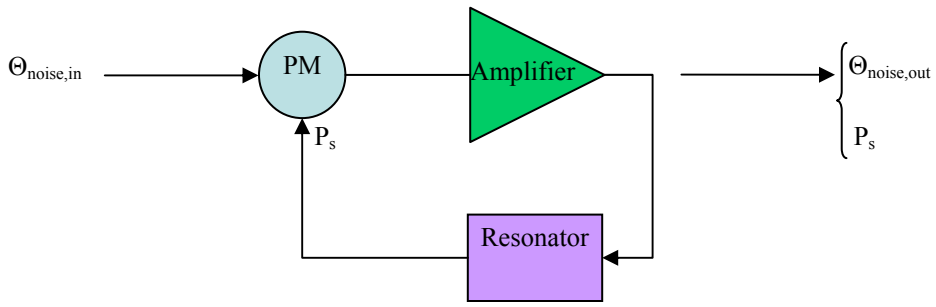


Fig. 6.3. Linear model for the phase-noise analysis of feedback oscillator

6.2.2 Linear Time-Variant (LTV) Model (Hajimiri's Model)

Since the oscillators are essentially time-varying, the time-variant approach seems to be a more appropriate approach in modeling the phase-noise. With this in mind, Hajimiri proposed a novel LTV phase-noise model for feedback oscillators [85]. The linear assumption for noise despite the obvious nonlinear large-signal behavior of the feedback system is justified when the noise power is much smaller than the carrier power.

The heart of this theory is based on the impulse sensitivity function (ISF). Time-varying perturbation results in time-varying phase fluctuations. The unit impulse response for excess phase of an oscillator can be expressed [85] as:

$$h_{\phi}(t,\tau)=\frac{\Gamma(2\pi f_0 t)}{q_{\max}}u(t-\tau), \tag{6.8}$$

where q_{max} is the maximum charge displacement on the node, u(t) is the unit step function, and Γ(x) is the impulse sensitivity function. The ISF is a dimensionless, frequency- and amplitude-independent periodic function with period equal to 2π. This function describes how much phase shift results from applying a unit impulse at time t=τ and is a function of the oscillation waveform. Skipping the details of the Fourier series analysis, one can show that the excess phase generated from ISF can be expressed by:

$$\phi(t) \approx \frac{I_n c_n \sin(\Delta\omega t)}{2q_{\max}\Delta\omega}, \tag{6.9}$$

where I_n and c_n are the current amplitude and coefficient for the n-th term in the Fourier series. To better understand the impact of excess phase on the oscillation spectrum, it is beneficial to understand the phase to voltage transformation mechanism in the oscillator. Fig. 6.4 shows a general block diagram of the LTV phase-noise model showing the phase-to-voltage converter. Note that the nonlinearities of the oscillator (both amplifier and micromechanical resonator) affect the ISF waveform and the oscillation waveform.

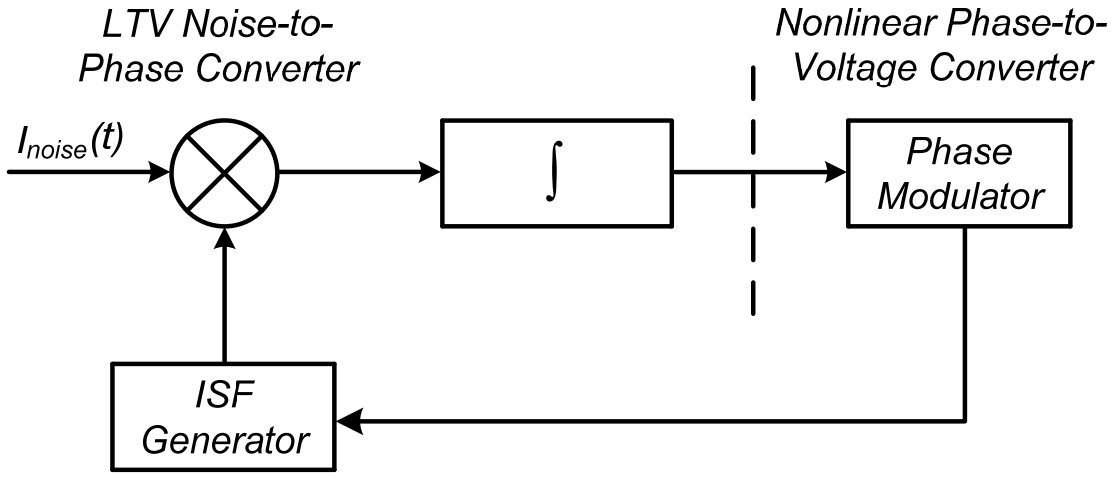


Fig. 6.4. General block diagram of the LTV phase-noise model

By computing the PSD of the oscillation waveform, the phase-noise can be obtained. The excess phase generated by an injected current at $n\omega_0+\Delta\omega$ results in double sideband power relative to carrier. The single sideband PSD is given by:

$$\frac{P_{out}}{P_s} = \left(\frac{I_n c_n}{4q_{\max}\Delta\omega}\right)^2. \tag{6.10}$$

Finally, when considering the contribution from thermal noise, a closed-form solution for the oscillator phase-noise in dB can be found:

$$L(\Delta\omega) = 10\log_{10}\left(\frac{\overline{i_n^2}\cdot\sum_{n=0}^{\infty} c_n^2}{4q_{\max}^2.\Delta\omega^3}\right). \tag{6.11}$$

Using Parseval's theorem, the expression for the phase-noise is simplified to:

$$L(\Delta\omega) = 10\log_{10}\left(\frac{\Gamma_{rms}^2}{q_{\max}^2}\cdot\frac{\overline{i_n^2}}{2q_{\max}^2.\Delta\omega^3}\right), \tag{6.12}$$

where Γ_{rms} is the RMS value of the ISF. If the contributions from flicker noise sources are considered, the overall close-to-carrier phase-noise performance can be approximated:

$$L(\Delta\omega) = 10\log_{10}\left[\left(\frac{\Gamma_{rms}^2}{q_{\max}^2}\cdot\frac{\overline{i_n^2}}{2q_{\max}^2.\Delta\omega^3}\right)+\left(\frac{c_0^2}{q_{\max}^2}\cdot\frac{\overline{i_n^2}}{4.\Delta\omega^3}\cdot\frac{\omega_c}{\Delta\omega}\right)\right], \tag{6.13}$$

where ω_c is the flicker noise corner frequency.

6.2.3 Nonlinear Time-Invariant (NLTI) Model (Samori's Model)

This model is based on a more practical nonlinear approach in modeling oscillators [87]. After all, the large-signal operation of an amplifier is synonymous to nonlinearity. The study of the NLTI model starts with finding the harmonic transfer function of oscillator with a pre-defined frequency selective tank. Then the single side-band PSD of the output noise voltage can be calculated to arrive at the final expression for the phase-noise of the oscillator. The phase-noise of the oscillator in $1/f^2$ region can be approximated by:

$$L(\Delta\omega) = \frac{2}{V_0^2}\cdot\frac{kT}{C}\cdot\frac{\omega_0}{Q}\cdot\frac{1}{\Delta\omega^2}(1+F), \tag{6.14}$$

where V_0 is the oscillation amplitude, Q is the quality factor of the resonating tank, and F is the nonlinear noise factor. Continuing with the nonlinear analysis of the output signal,

V(t), it is possible to have a more accurate expression for "F" based on other known parameters in the circuit.

6.3 Sources of Phase-Noise in Micromechanical Oscillators

The noise sources for micromechanical oscillators are categorized into two groups: electronic and mechanical noise sources. Electronic noise sources are well-known. They include thermal and flicker noise of the active and passive devices used in the oscillation block. This includes the noise contribution of circuits that are outside the feedback loop such as ALC [82]. The noise from control block such as temperature/process compensation circuit and tuning control signal supplied by the PLL indirectly contribute to the overall phase-noise; the noise from these blocks is modulated by the frequency vs. tuning transfer function of tuning circuit before showing up in the phase-noise of the micromechanical oscillator.

The main source of mechanical noise is the micromechanical resonator. The mechanical noise that is usually low frequency in the resonator originates from two sources: first, the nonlinearity of the micromechanical resonator. The resonator is driven into nonlinearity due to its limited power handling capability and nonlinearity of the transducer [83].

The power handling is mostly limited by the nonlinearity mechanisms in the resonator. In a linear mass-spring system the spring coefficient is a constant where as in a nonlinear system, the spring coefficient does not linearly change with the displacement [30]. A nonlinear spring coefficient will cause larger harmonics of the natural resonance

frequency, ω_0, to appear in the output. Consequently, the resonance frequency is dependent on the vibration amplitude [88].

The nonlinearity of the electromechanical transducers whether capacitive [6] or piezoelectric [30] contributes to the noise of the micromechanical resonator. In capacitive resonators, the noise aliasing from the polarization voltage further deteriorates the close-to-carrier phase-noise performance.

The other major noise source in a micromechanical resonator is due to random low frequency vibrations that is possibly caused by particle adsorption and desorption.

6.4 LTI Phase-Noise Model for Series-Resonant Lateral MEMS Oscillators

To be able to improve the phase-noise performance of the micromechanical oscillators, it is necessary to have a good understanding of the phase-noise mechanism and derive analytical models that are in good agreement with measurement data. This modeling work will be considered a significant step forward toward creating an advanced systematic design methodology for the design and optimization of high frequency micromechanical oscillators.

While the LTI classical phase noise theory [84] provides reasonable phase noise estimates for crystal type oscillators, the presence of resonator parasitics reduces its value as comprehensive and accurate analytical phase-noise model for micromechanical oscillators. The problem is more severe for classical phase-noise theories such a Leeson's [81] that require curve fitting to obtain the empirical parameters. Although Hajimiri's

model [85], [86] offers an IC designer a much-needed insight into the factors affecting empirical parameters by providing a more realistic LTV approach, the mere complexity of this approach diminishes its prospect as the comprehensive oscillator phase-noise theory. The difficulty in finding the relationship between the ISF and nonlinearity mechanism of the resonator adds to this complexity for micromechanical oscillators. The same argument can be made for NLTI approach where the impact of nonlinearity modeling is more pronounced on the accuracy of the phase-noise model.

In this study, we focus on the LTI approach that is the simplest model among the ones discussed in section 6.2. The inefficiency of the LTI approach including its poor accuracy is compensated by modifying the model to include the effect of the resonator and amplifier parasitic impedances.

6.4.1 LTI Model for Oscillator with Ideal Lateral MEMS Resonator

As described earlier, the LTI theory predicts that the PSD of the output noise of a feedback oscillator is equal to PSD of the input noise multiplied by the closed-loop gain of the oscillator. Considering major electronic noise sources of an amplifier, i.e. thermal and flicker noise, the PSD of the input noise is given by (6.5). Finding the transfer function of the micromechanical resonator which acts as the frequency selective tank and expressing it in terms of known parameters such as Q and R_m, is the precursor to determining the closed-loop gain of the oscillator. The resonator transfer function can be written in terms of the Q of the resonator [84]:

$$H(f_m) = \frac{1}{1 + j\left(2Q\frac{f_m}{f_0}\right)}, \tag{6.15}$$

where f_m and f_0 are the offset and career frequency, respectively. Once the resonator transfer function is available, the closed-loop transfer function of feedback system can be easily found:

$$\left|G_{noise}(f_m)\right|^2 = 1 + \frac{1}{f_m^2}\left(\frac{f_0}{2Q}\right)^2 . \tag{6.16}$$

Substituting (6.16) in (6.7) and assuming half of the noise spectrum is modulated as phase-noise, the output phase-noise can be derived as:

$$L(f_m) = 10\log_{10}\frac{kTF}{2P_s}\left(1+\frac{f_c}{f_m}\right)\left[1+\frac{1}{f_m^2}\left(\frac{f_0}{2Q}\right)^2\right]. \tag{6.17}$$

Note that the equation (6.17) does not predict the impact of the mechanical noise of the phase-noise performance of the micromechanical oscillator. From this analysis, the major impact of the micromechanical resonator on the oscillator phase-noise performance comes only through the Q; the higher the Q of the resonator, the better the close-to-carrier phase-noise performance.

6.4.2 LTI Approximation of the 1st-Order Parasitic Effects on the Phase-Noise

The aforementioned analysis is only valid for oscillators made with ideal amplifier and micromechanical resonators. In reality, however, both of these blocks have considerable parasitics associated with them. At the beginning, we consider the first-order parasitic effects on the phase-noise performance. Let's assume a non-ideal amplifier with input resistance, R_{in}, and output resistance, R_{out}, is placed in shunt feedback with a series-resonant micromechanical resonator with motional resistance, R_m, and unloaded Q, Q_{res}, to make an oscillator (Fig. 6.5). The effect of these amplifier and resonator parasitic

impedances can be considered in the form of Q loading. The resonator transfer function should be modified to account for loss that is modeled by the motional resistance:

$$H(f_m) = \frac{1}{R_m\left[1 + j\left(2Q\frac{f_m}{f_0}\right)\right]}. \tag{6.18}$$

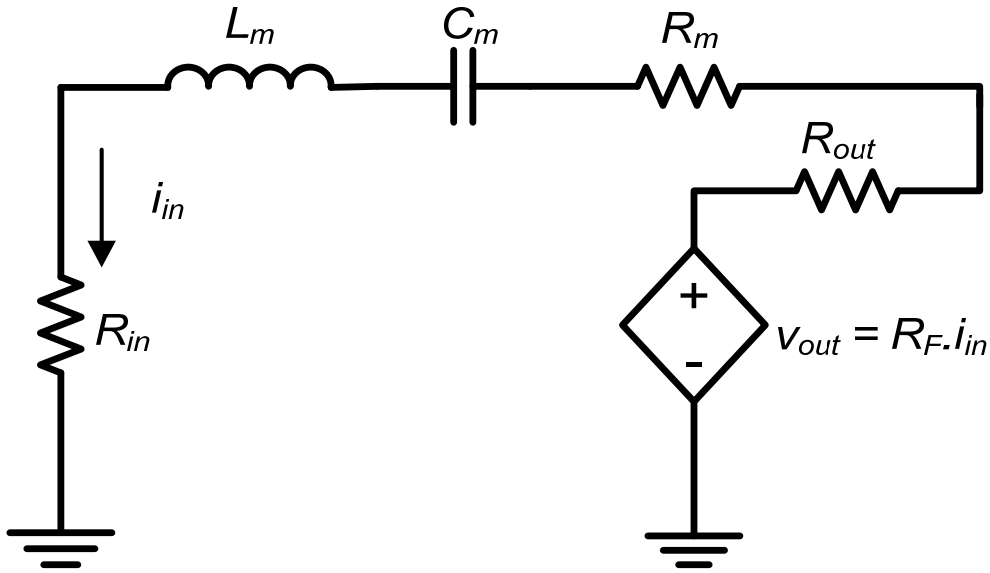


Fig. 6.5. Equivalent model with 1st-order parasitics for series-resonant oscillator

Since the micromechanical resonator is modeled as a series RLC tank, a more appropriate transfer function would be the ratio between the output current to the input voltage to the resonator, R_{tank}:

$$R_{\tan k}(f_m) = R_m\left[1 + j\left(2Q\frac{f_m}{f_0}\right)\right]. \tag{6.19}$$

Using equation (6.19), the loop transfer function, G_{noise}, can be expressed as:

$$G_{noise}(f_m) = \frac{v_{out}(f_m)}{i_{in}(f_m)} = \frac{R_F}{1 - \frac{R_F}{R_{in} + R_{out} + R_{\tan k}(f_m)}}, \tag{6.20}$$

where R_F is the transimpedance gain of the TIA. Using the closed-loop transfer function and considering the effect of amplifier loading on the resonator, the phase-noise of the micromechanical oscillator can be calculated:

$$L(f_m) = 10\log_{10}\frac{kTF}{2P_s}\left(1+\frac{f_c}{f_m}\right)\left[1+\frac{1}{f_m^2}\left(\frac{f_0}{2Q_L}\right)^2\right], \tag{6.21}$$

where Q_L is the loaded Q of the resonator and is given by:

$$Q_L = \frac{R_m}{R_{in}+R_{out}+R_m}Q. \tag{6.22}$$

Equation (6.22) clearly shows the Q reduction due to the finite input and output resistance of the TIA.

6.4.3 LTI Approximation of the 2nd-Order Parasitic Effects on the Phase-Noise

While considering the first-order parasitic impedances of the TIA and micromechanical resonator certainly improves the accuracy of the LTI phase-noise model, the predicted phase-noise performance of high frequency micromechanical oscillators remains significantly underestimated when compared with the measurement. The most important reason behind this discrepancy is second-order parasitic effects from both the TIA and micromechanical oscillator. These parasitic effects include shunt and feedthrough parasitic capacitances of the micromechanical resonator in addition to the input and output reactance of the TIA. Since the feedthrough capacitance of lateral micromechanical resonators is small (<10fF), it can be safely ignored in this analysis.

Fig. 6.6 shows the equivalent circuit for phase-noise calculation when both first-order and second-order parasitic impedances are considered. Due to the fact that the operating

frequency is usually significantly lower than the f_T of the IC technology in the specific biasing situation, the input and output impedances of the TIA are modeled as an RC network rather than an RLC. Similar to analysis given in section 6.4.2, the first step is to find the closed-loop transfer function of the feedback system. The closed-loop gain of the feedback system is then used to find the PSD of the output noise and consequently the phase-noise of the oscillator.

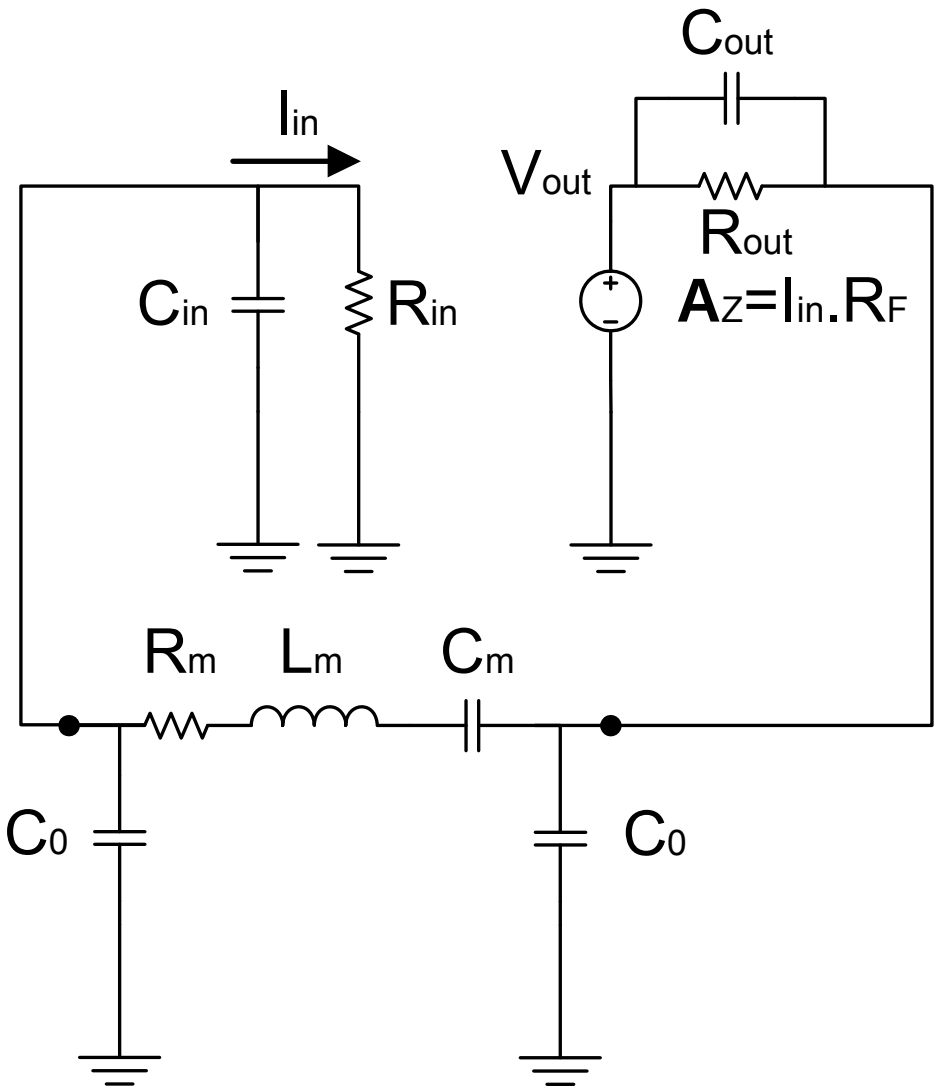


Fig. 6.6. Equivalent model with 2nd-order parasitics for series-resonant oscillator

Solving the network of Fig. 6.6 for v_{out}/i_{in}, the closed-loop transfer function of the feedback oscillator is obtained:

$$\left.\begin{aligned} i_{in} &= i_{noise} + \frac{v_{out}}{Z_{out} + Z_{eq}} \\ v_{out} &= R_F . i_{in} \\ Z_{out} &= R_{out} \left\| \frac{1}{C_{out}.s} \right. \\ Z_{in} &= R_{in} \left\| \frac{1}{C_{in}.s} \right. \\ Z_{eq} &= \left[\left(Z_{in}.s \left\| \frac{1}{C_0.s} \right. \right) + R_{\tan k} \right] \left\| \frac{1}{C_0.s} \right. \end{aligned} \right\} \rightarrow \frac{v_{out}}{i_{in}} = R_F . \frac{Z_{out} + Z_{eq}}{Z_{out} + Z_{eq} - R_F} \qquad (6.23)$$

where R_{tank} is the transfer function of micromechanical resonator. Equation (6.23) can be simplified if input and output capacitance of the TIA, C_{in} and C_{out}, are assumed to be much smaller C_0. This is a valid assumption as the ever-shrinking device feature size in advanced CMOS processes help reduce the parasitic capacitance of the MOS devices which are the major contributor to the input and output capacitance of the TIA. C_{in} of the TIA appear in parallel with C_0 and can be easily absorbed into C_0. Similarly, the equivalent capacitance at the output node can be approximated by the much-larger C_0 of the micromechanical resonator:

$$\begin{aligned} C_{in} << C_0 \Rightarrow C_{in} + C_0 \approx C_0, Z_{in} \approx R_{in} \\ C_{out} << C_0 \Rightarrow C_{out} + C_0 \approx C_0, Z_{out} \approx R_{out} \end{aligned} . \qquad (6.24)$$

With this assumption, the Z_{eq} is reduced to:

$$Z_{eq}(j\omega) = \frac{R_{\tan k}\left(1 + j.R_{in}.C_0.\omega\right) + R_{in}}{j.R_{\tan k} C_0 \omega\left(1 + j.R_{in}.C_0.\omega\right) + 2\left(1 + j.R_{in}.C_0.\omega\right) - 1} . \qquad (6.25)$$

We can now find the closed-loop transfer function, G_{noise}:

$$G_{noise}(j\omega)=\frac{v_{out}}{i_{in}}=R_F\left[\frac{R_{\tan k}(1+jR_{out}.C_0.\omega)+R_{in}+R_{out}}{R_{\tan k}(1+jR_{out}.C_0.\omega)+R_{in}+R_{out}-R_F(1+j.R_{\tan k}.C_0\omega)}\right]. \quad (6.26)$$

Z_{eq} and G_{noise} can be further simplified for TIAs with large BW that are natural choice to ensure minimal extra phase-shift due to presence of the sustaining amplifier in the oscillation loop. This assumption is more general and requires small input and output impedance; this mean both small resistance and capacitance at critical nodes such as the input and output. With this assumption, Z_{eq} is given by:

$$TIA\big|_{BW} >> \omega_{res} \Rightarrow |j.R_{in}.C_0\omega| << 1 \Rightarrow Z_{eq}(j\omega)=\frac{R_{\tan k}+R_{in}}{1+j.R_{\tan k}.C_0\omega}. \quad (6.27)$$

We can now find the closed-loop transfer function, G_{noise}:

$$\begin{gathered} TIA\big|_{BW} >> \omega_{res} \Rightarrow |j.R_{out}.C_0\omega| << 1 \\ \Rightarrow G_{noise}(j\omega)=R_F\left[\frac{R_{\tan k}+R_{in}+R_{out}}{R_{\tan k}+R_{in}+R_{out}-R_F(1+j.R_{\tan k}.C_0\omega)}\right] \end{gathered} \quad (6.28)$$

The next step is to express the G_{noise} in terms of known parameters such as the Q and R of the micromechanical resonator. The oscillation frequency in the presence of shunt parasitic capacitances of the resonator can be approximated by:

$$\omega_{osc}=\frac{1}{\sqrt{L_mC_m}}\sqrt{1+\frac{2C_m}{C_p}}, \quad (6.29)$$

where L_m is the equivalent motional inductance of the micromechanical resonator. Since $C_m << C_p$, the oscillation frequency is very close to the natural resonance frequency of the micromechanical resonator, i.e. $\omega_{osc} \approx \omega_{res}$. Having said that, G_{noise}, can be approximated by:

$$G_{noise}(j\omega) \approx R_F \frac{R_{in} + R_{out} + R_m.\left[1 + 2j.Q_{res}\left(\frac{\omega_m}{\omega_{osc}}\right)\right]}{R_{in} + R_{out} - R_F + R_m.\left[1 - j.R_F.C_0.\omega_m\right].\left[1 + 2j.Q_{res}\left(\frac{\omega_m}{\omega_{osc}}\right)\right]}, \quad (6.30)$$

where Q_{res} is the unloaded Q of the micromechanical resonator. To find the PSD of the output noise, the next step is to find $|G_{noise}|^2$:

$$|G_{noise}(j\omega)|^2 \approx R_F^2. \left\{ \frac{\left[R_{total}.(R_{total} - R_F) + 2R_m.R_F.Q_{res}.C_0.\left(\frac{\omega_m^2}{\omega_{osc}}\right).(R_{total} - R_m) + 4R_m^2.Q_{res}^2.\left(\frac{\omega_m}{\omega_{osc}}\right)^2\right]^2}{\left\{\left(R_{total} - R_F + 2R_F R_m.C_0.\left(\frac{\omega_m^2}{\omega_{osc}}\right)\right)^2 + R_m^2\left(2Q_{res}\left(\frac{\omega_m}{\omega_{osc}}\right) - R_F.C_0.\omega_m\right)^2\right\}^2} + \frac{R_m^2.R_F^2.\left[R_{total}.C_0\omega_m - 2Q_{res}.\left(\frac{\omega_m}{\omega_{osc}}\right) + 4R_m.C_0.Q_{res}^2.\omega_m.\left(\frac{\omega_m}{\omega_{osc}}\right)^2\right]^2}{\left\{\left(R_{total} - R_F + 2R_F R_m.C_0.\left(\frac{\omega_m^2}{\omega_{osc}}\right)\right)^2 + R_m^2\left(2Q_{res}\left(\frac{\omega_m}{\omega_{osc}}\right) - R_F.C_0.\omega_m\right)^2\right\}^2} \right\} \quad (6.31)$$

where $R_{total}=R_{in}+R_{out}+R_m$. Then, the phase-noise of the oscillator is given by:

$$L(\omega_m) \approx \frac{1}{2}.\frac{kT_0F}{P_S}.\left(1 + \frac{\omega_c}{\omega_m}\right). \left\{ \frac{\left[R_{total}.(R_{total} - R_F) + 2R_m.R_F.Q_{res}.C_0.\left(\frac{\omega_m^2}{\omega_{osc}}\right).(R_{total} - R_m) + 4R_m^2.Q_{res}^2.\left(\frac{\omega_m}{\omega_{osc}}\right)^2\right]^2}{\left\{\left(R_{total} - R_F + 2R_F R_m.C_0.\left(\frac{\omega_m^2}{\omega_{osc}}\right)\right)^2 + R_m^2\left(2Q_{res}\left(\frac{\omega_m}{\omega_{osc}}\right) - R_F.C_0.\omega_m\right)^2\right\}^2} + \frac{R_m^2.R_F^2.\left[R_{total}.C_0\omega_m - 2Q_{res}.\left(\frac{\omega_m}{\omega_{osc}}\right) + 4R_m.C_0.Q_{res}^2.\omega_m.\left(\frac{\omega_m}{\omega_{osc}}\right)^2\right]^2}{\left\{\left(R_{total} - R_F + 2R_F R_m.C_0.\left(\frac{\omega_m^2}{\omega_{osc}}\right)\right)^2 + R_m^2\left(2Q_{res}\left(\frac{\omega_m}{\omega_{osc}}\right) - R_F.C_0.\omega_m\right)^2\right\}^2} \right\} \quad (6.32)$$

For feedback oscillators in the steady-state condition (unity gain), the transimpedance gain, R_F, is almost equal to total loss from the resonator and the amplifier, i.e. R_{total}. Now for close-to-carrier frequencies where $\omega_m << \omega_{osc}$, the phase-noise can be further simplified to:

$$L(\omega_m) \approx \frac{1}{2}.\frac{kT_0F}{P_S}.\left(1+\frac{\omega_c}{\omega_m}\right).$$
$$\left\{\begin{array}{l} \dfrac{\left[2R_m.R_{total}.Q_{res}.C_0.\left(\dfrac{\omega_m^2}{\omega_{osc}}\right).(R_{total}-R_m)+4R_m^2.Q_{res}^2.\left(\dfrac{\omega_m}{\omega_{osc}}\right)^2\right]^2}{\left\{\left(2R_{total}R_m.C_0.\left(\dfrac{\omega_m^2}{\omega_{osc}}\right)\right)^2+R_m^2\left(2Q_{res}\left(\dfrac{\omega_m}{\omega_{osc}}\right)-R_{total}.C_0.\omega_m\right)^2\right\}^2} \\ +\dfrac{R_m^2.R_{total}^2.\left[R_{total}.C_0\omega_m-2Q_{res}.\left(\dfrac{\omega_m}{\omega_{osc}}\right)+4R_m.C_0.Q_{res}^2.\omega_m.\left(\dfrac{\omega_m}{\omega_{osc}}\right)^2\right]^2}{\left\{\left(2R_{total}R_m.C_0.\left(\dfrac{\omega_m^2}{\omega_{osc}}\right)\right)^2+R_m^2\left(2Q_{res}\left(\dfrac{\omega_m}{\omega_{osc}}\right)-R_{total}.C_0.\omega_m\right)^2\right\}^2} \end{array}\right\}. \quad (6.33)$$

The expression for phase-noise looks rather complicated. To better understand the effect of second-order parasitics on the phase-noise, it is beneficial to look into several particular cases and then use computer-aided programs such as MATLAB to accurately approximate the oscillator phase-noise.

- Very small C_0 ($C_0 \approx 0$):

For very small C_0, the equation (6.33) can be reduced to a form similar to (6.21), in effect eliminating neglecting the effect of second-order parasitics. For reasons stated earlier, the accuracy of this model is greatly compromised for high frequency lateral micromechanical resonators. Even if the resonator shunt parasitic is reduced, the mere presence of input/output parasitic of the amplifier makes the performance worse and renders the first-order model incapable of providing accurate phase-noise approximation.

- Very large R_m ($R_m >> R_{in} + R_{out}$):

When motional resistance is very large, the Q loading effect due to the amplifier parasitic becomes insignificant. As such, the total resistance, R_{total}, can be approximated by R_m and the equation (6.33) can be simplified to:

$$L(\omega_m) \approx \frac{1}{2}.\frac{kT_0F}{P_S}.\left(1+\frac{\omega_c}{\omega_m}\right). \left\{ \frac{16R_m^4.Q_{res}^4.\left(\frac{\omega_m}{\omega_{osc}}\right)^4}{\left\{4R_m^4.C_0^2.\left(\frac{\omega_m^2}{\omega_{osc}}\right)^2+R_m^2\left(2Q_{res}\left(\frac{\omega_m}{\omega_{osc}}\right)-R_m.C_0.\omega_m\right)^2\right\}^2} + \frac{R_m^4.\left[R_m.C_0\omega_m-2Q_{res}.\left(\frac{\omega_m}{\omega_{osc}}\right)+4R_m.C_0.Q_{res}^2.\omega_m.\left(\frac{\omega_m}{\omega_{osc}}\right)^2\right]^2}{\left\{4R_m^4.C_0^2.\left(\frac{\omega_m^2}{\omega_{osc}}\right)^2+R_m^2\left(2Q_{res}\left(\frac{\omega_m}{\omega_{osc}}\right)-R_m.C_0.\omega_m\right)^2\right\}^2} \right\}. \quad (6.34)$$

This is the near minimum phase-noise that can be achieved with an ideal TIA with infinitely-small input and output impedance (and consequently very large BW), i.e. no loading effect from the amplifier.

Turning into a powerful CAD tool such as MATLAB, it is possible to see the effect of variation in shunt parasitic capacitance on the phase-noise performance of the oscillator. Fig. 6.7 shows the predicted phase-noise of a typical 1GHz lateral piezoelectric micromechanical oscillator when the shunt parasitic capacitance of the resonator, C_0, is varied between 0.5pF to 4pF. The phase-noise performance clearly gets worse with large shunt parasitic capacitance.

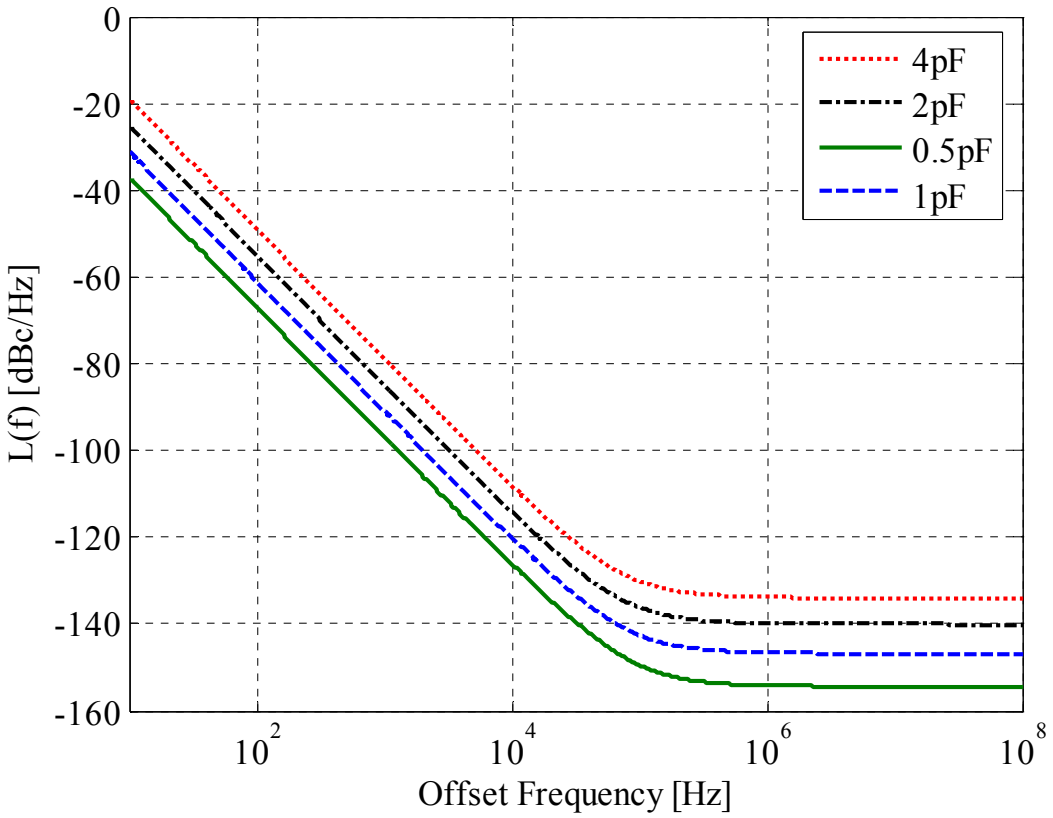


Fig. 6.7. Variation in phase-noise performance with C_p

6.5 Case Study

After developing an analytical LTI phase-noise model for lateral micromechanical oscillators, it is necessary to validate the model with measured phase-noise data. Since the characteristics of the lateral piezoelectric and capacitive micromechanical resonator differ (especially Q and R_m), it is logical to bring examples of each type of the micromechanical oscillator and separately study the application of the aforementioned phase-noise model in each case.

Both LTI phase-noise models, one that only considers the effect of first-order parasitics and another one that takes into the account the effect of second-order parasitics are used

in this process. The goal is to determine the accuracy of the LTI phase-noise model with second-order parasitics included by comparing it with the measured phase-noise data and the LTI model that only considers first-order parasitic effects. When applying the LTI phase-noise model to the measured data, the empirical parameters such as "F" are chosen based on the measured data and kept fixed throughout this process for both first-order and second-order approximation.

6.5.1 High-frequency capacitive micromechanical oscillator

Capacitive micromechanical resonators usually offer high Q but they exhibit larger loss than piezoelectric micromechanical resonators with similar resonance frequency. This study envisions a capacitive SiBAR as the frequency selective tank. High frequency capacitive SiBARs exhibit motional resistance in the range of 1kΩ to over 10kΩ with Q in excess of 10,000 [12]. For this work, we use a 97MHz SiBAR with $Q_{operating}$≈40,000, R_m≈5kΩ, and V_p≈16V (Fig. 6.8).

The 97MHz SiBAR is interfaced with a low-power two-stage TIA to sustain the oscillation. The oscillation is sustained at V_P≈16V with output power around 3dBm (after gain of +10dB from the buffer). The measured phase-noise is better than -112dBc/Hz at 1kHz offset with floor reaching -135dBc/Hz (Fig. 6.9). The phase-noise floor can be improved by reducing the motional resistance of the SiBAR that is easily achieved by applying larger V_p; however, due to the small gap size, this comes at the expense of potentially pushing the capacitive transducer into nonlinear region and negatively affecting the close-to-carrier phase-noise performance of the oscillator.

The next step is to apply the LTI model that was derived in previous section to the measured phase-noise data and investigate the parasitic effects on the phase-noise. Fig. 6.10 shows the measured phase-noise of the 97MHz capacitive SiBAR oscillator with two lines showing the fitted LTI phase-noise models. The black line phase-noise approximation only considers the effect of first-order parasitic impedances, i.e. finite input/output resistance of the amplifier and non-zero motional resistance of the SiBAR. The green line represents the phase-noise model that takes into the account both the first-order and second-order non-idealities of the amplifier and micromechanical resonator. In both cases, the empirical parameters such as "F" are kept constant. Form Fig. 6.10, it is clear that the green line representing the model with second-order parasitics is a better fit to the measured phase-noise in both close-to-carrier and far-from-carrier regions.

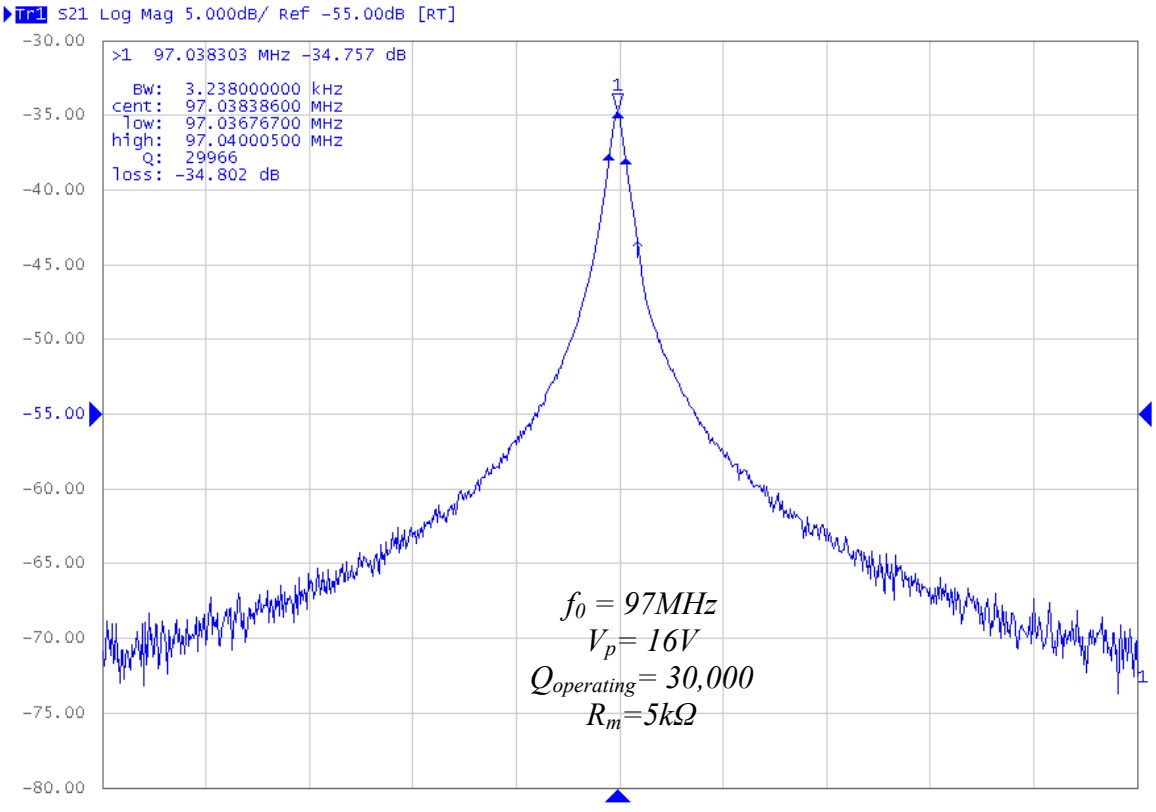


Fig. 6.8. Frequency response of the 97MHz capacitive SiBAR

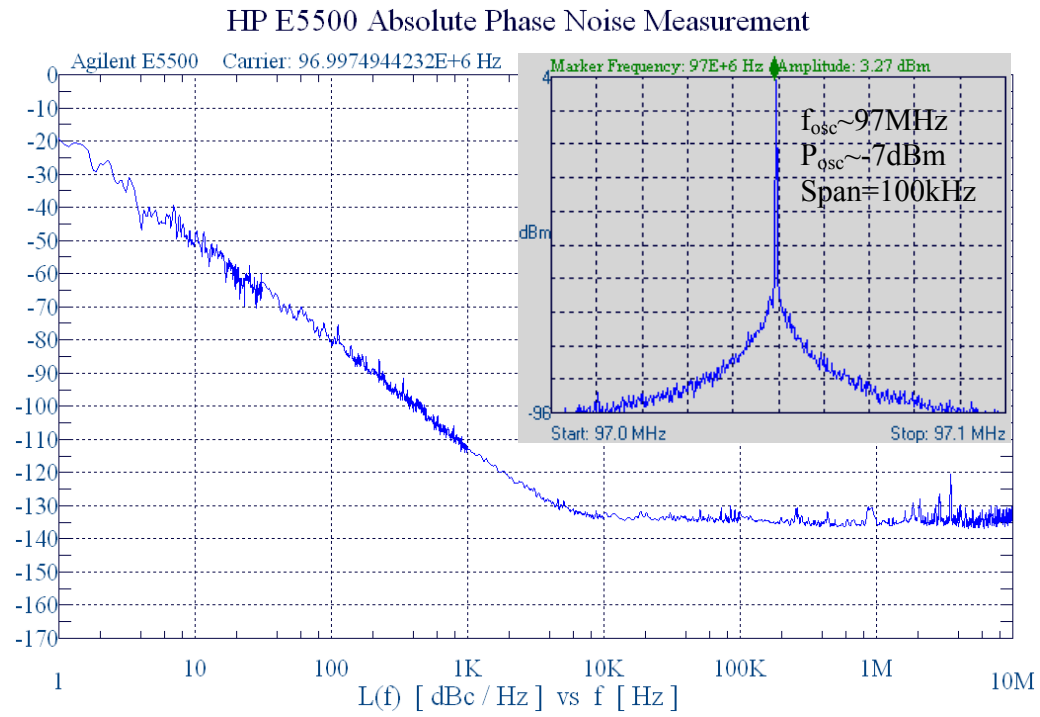


Fig. 6.9. Output spectrum and phase-noise of the 97MHz capacitive oscillator

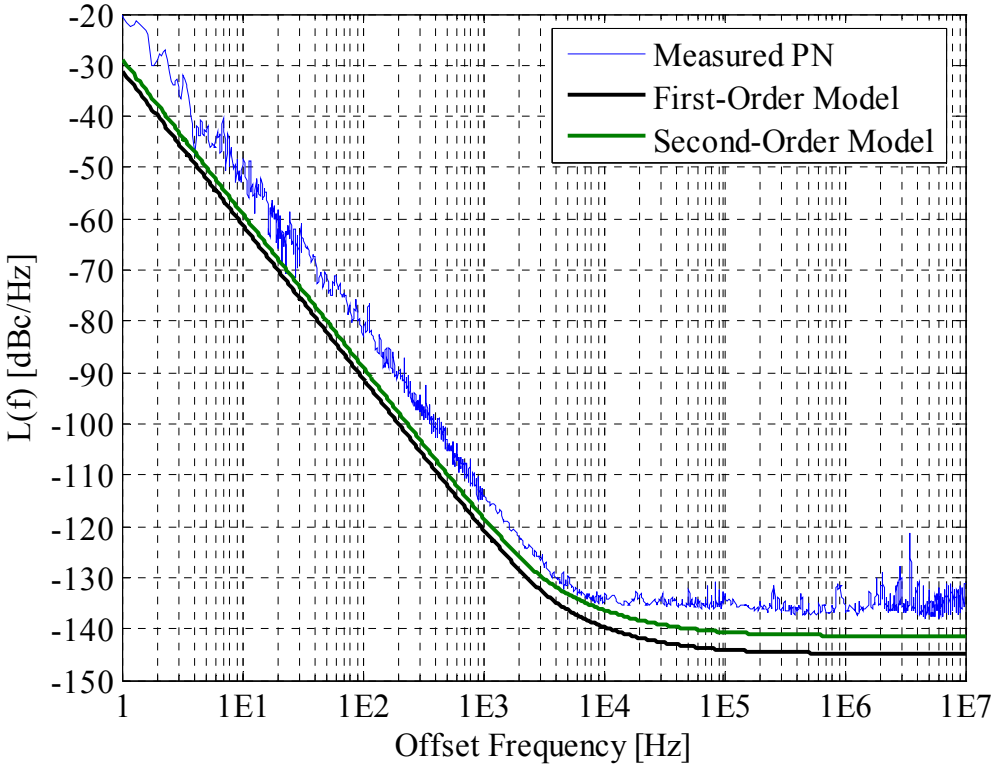


Fig. 6.10. 1st- and 2nd-order model fit to the phase-noise of the 97MHz oscillator

6.5.2 High-frequency lateral piezoelectric micromechanical oscillators

The main motivation behind using lateral piezoelectric micromechanical resonators is to facilitate the realization of low-power high frequency micromechanical reference oscillators in gigahertz range [66]. In this section, we focus on TPOS resonators for their higher Q and power handling both of which enhance the phase-noise performance of the oscillator. High-order TPOS resonators with motional resistance in the range of 100Ω to 1kΩ and unloaded Q larger than 1000, have been successfully reported in the literature [7]. For this work, we use two TPOS resonators, a 9th-order 463MHz AlN-on-Si resonator with $Q_{unloaded}$≈3,600, R_m≈200Ω that uses a very thin silicon oxide layer for TCF reduction (Fig. 6.11) and the 21st-order 1.006GHz AlN-on-Si resonator with large shunt parasitic capacitance, C_p~3.2pF, that was introduced in chapter 3 (Fig. 6.12).

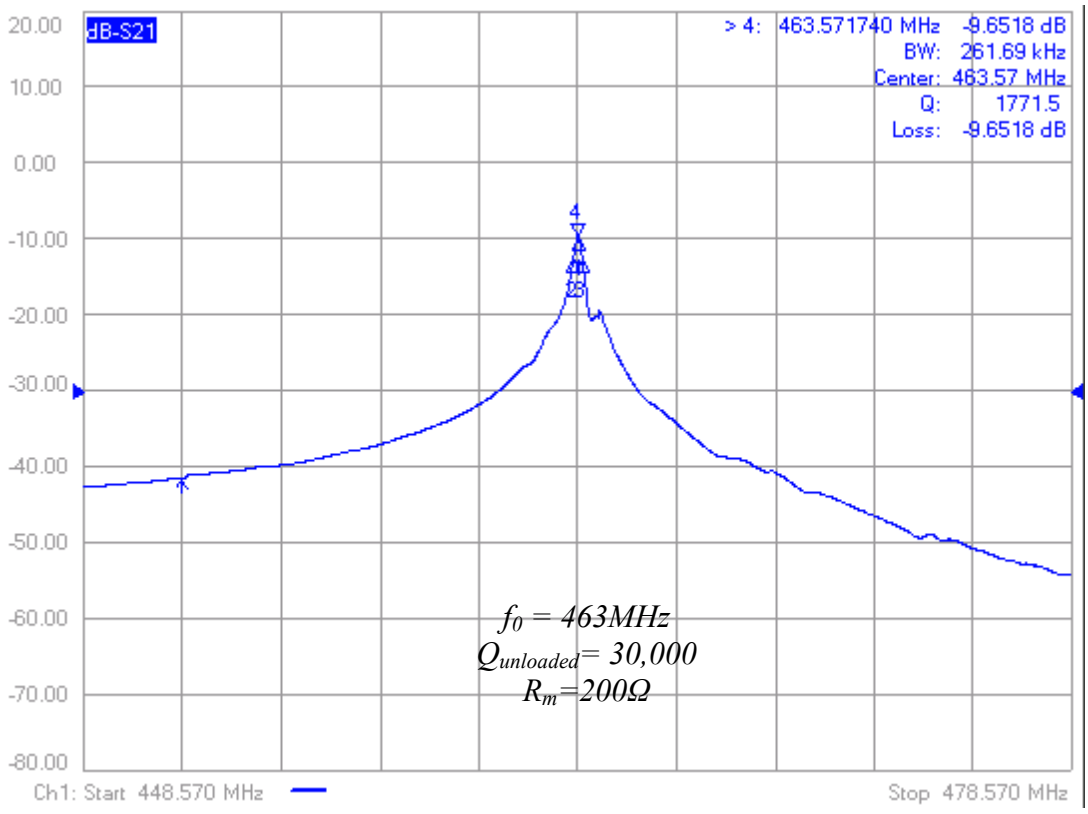


Fig. 6.11. Frequency response of the 463MHz TPOS resonator

The 463MHz AlN-on-Si micromechanical resonator is interfaced with a low-power three-stage TIA similar to the one shown in [7] to sustain the oscillation. The oscillation power is around -5dBm. The measured phase-noise is better than -90dBc/Hz at 1kHz offset with floor reaching -153dBc/Hz (Fig. 6.13). The 1.006GHz micromechanical oscillator is based uses the same sustaining amplifier that was described in chapter 3 with phase-noise better than -94dBc/Hz at 1kHz offset and floor around -154dBc/Hz (Fig. 3.41). The power of the oscillation is close to -3dBm.

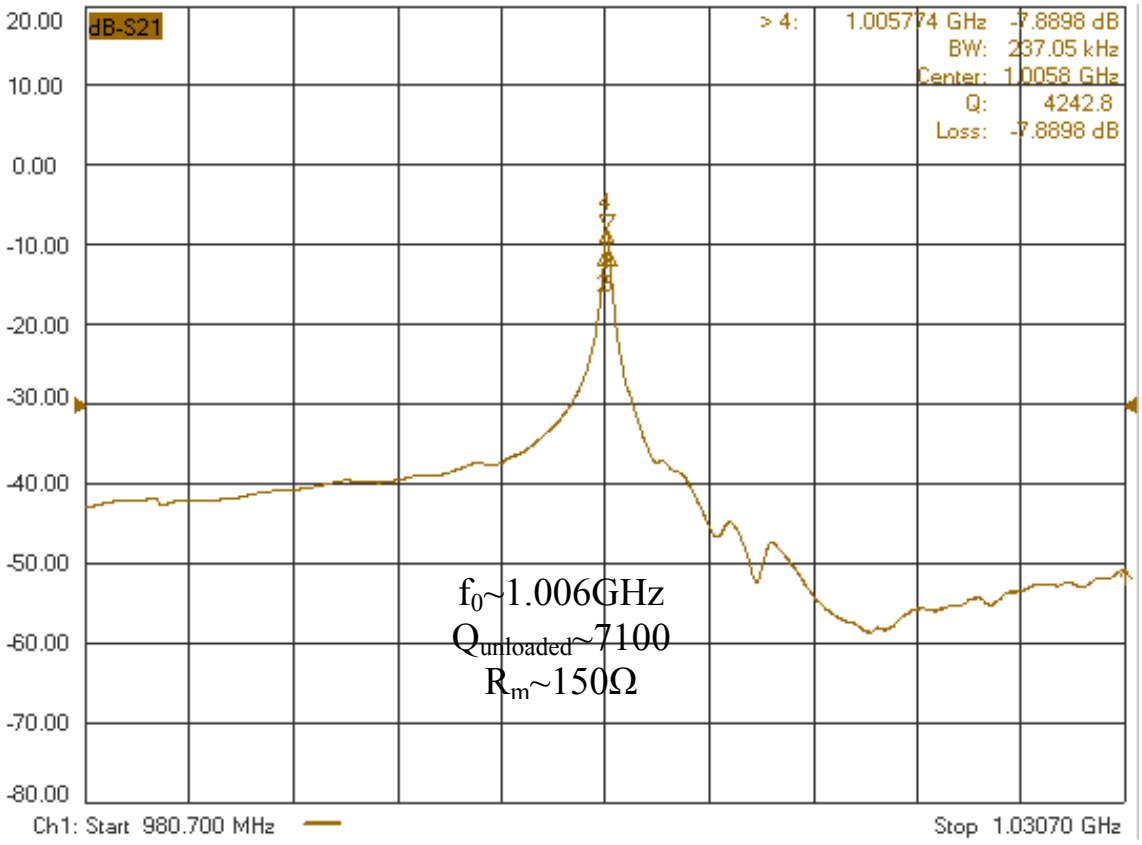


Fig. 6.12. Frequency response of the 1.006GHz TPOS resonator

Similar to the previous case, both first-order and second-order LTI models are fitted to the measured phase-noise data (Fig. 6.14 and 6.15). In both cases, the empirical parameters such as “F” are kept constant. The comparison of the fitted curves reveals that the phase-noise approximation by the second-order LTI model that takes into the account

both the first-order and second-order parasitic effects is much more accurate than the approximation done with the first-order LTI phase-noise model.

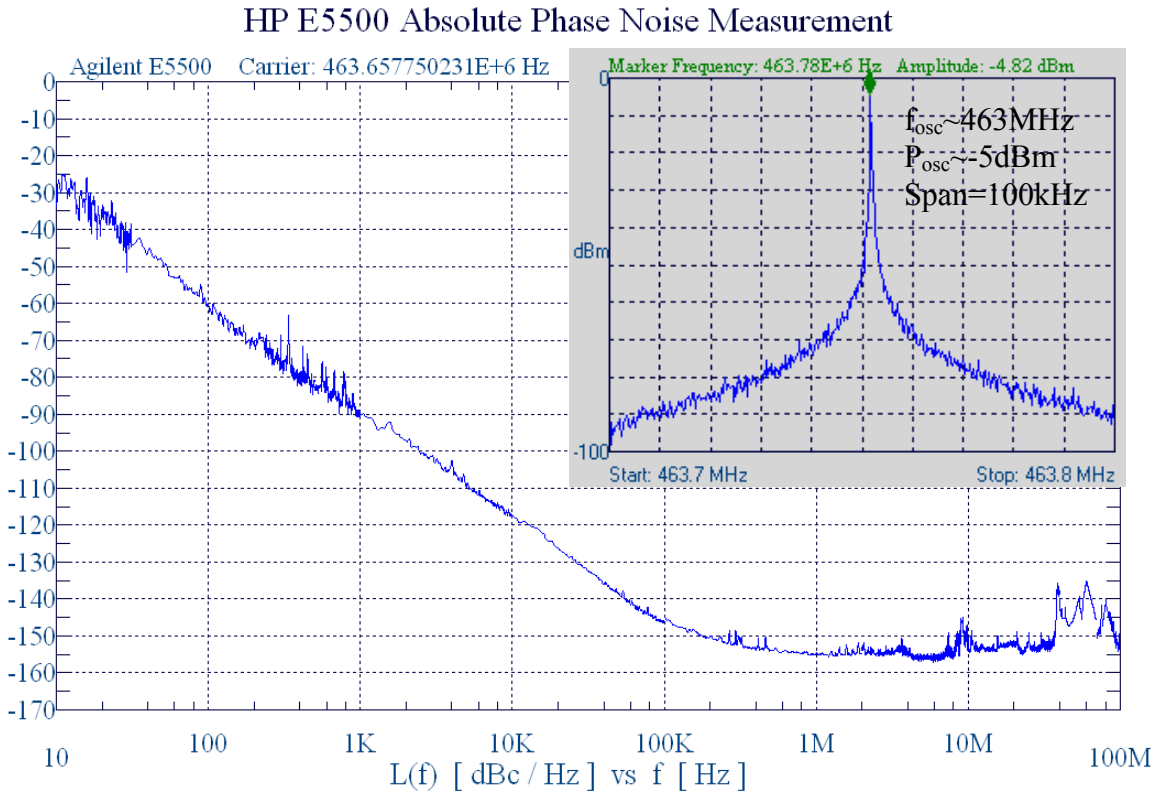


Fig. 6.13. Output spectrum and phase-noise of the 463 MHz AlN-on-Si oscillator.

The results in Fig. 6.14 and 6.15 highlight the effects of shunt parasitics as the oscillation frequency increases toward the UHF. A detailed comparison of fitted model results in Fig. 6.10, 6.14, and 6.15 show that as the frequency increases, the accuracy of the first-order LTI phase-noise model is reduced; while for 97MHz capacitive SiBAR oscillator, the first-order approximation is still a viable approach, the first-order phase-noise approximation of the 463MHz and 1.006GHz AlN-on-Si micromechanical oscillator are at least 10dB off from the measured values. From the results obtained in MATLAB for the second-order LTI model of the 463MHz and 1.006GHz oscillators, C_0~1pF is

probably the reasonable threshold when the first-order LTI phase-noise model should be dumped in favor of the more accurate second-order LTI model.

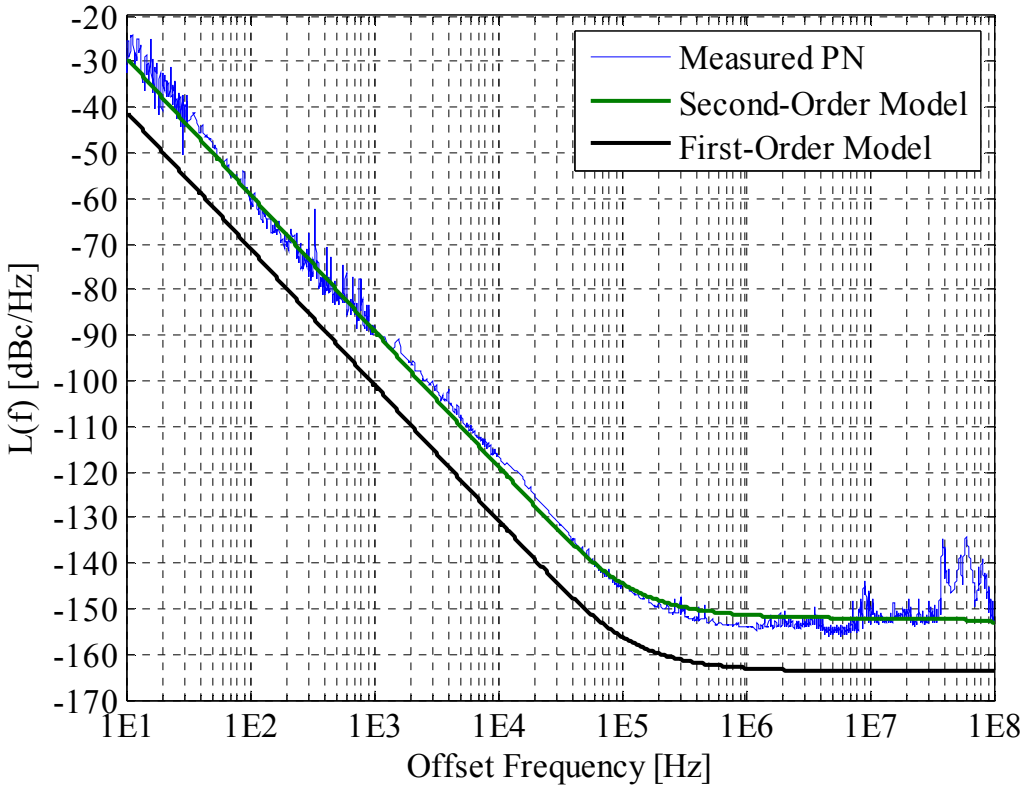


Fig. 6.14. 1st- and 2nd-order model fit to the phase-noise of the 463MHz oscillator

6.6 Conclusion

The phase-noise optimization and eventual improvement of micromechanical oscillators is hindered by the lack of comprehensive phase-noise modeling for such oscillators. Several electronic and mechanical noise sources contribute to the phase-noise of high-frequency lateral micromechanical oscillators, however, the main contributor to close-to-carrier phase-noise are flicker and thermal noise. Several well-known phase-noise models have been developed for predicting the phase-noise behavior of oscillator. Among them, the LTI model has a descent track record in predicting the phase-noise of quartz crystal

oscillators. Despite this relative success, their accuracy in predicting the phase-noise performance of high-frequency lateral micromechanical oscillator is considered marginal at best. This is partly due to the second-order parasitic effect from both the resonator and amplifier. Upon including these parasitics, the accuracy of the LTI phase-noise model is dramatically improved. This is supported by measurement data from high frequency micromechanical oscillators.

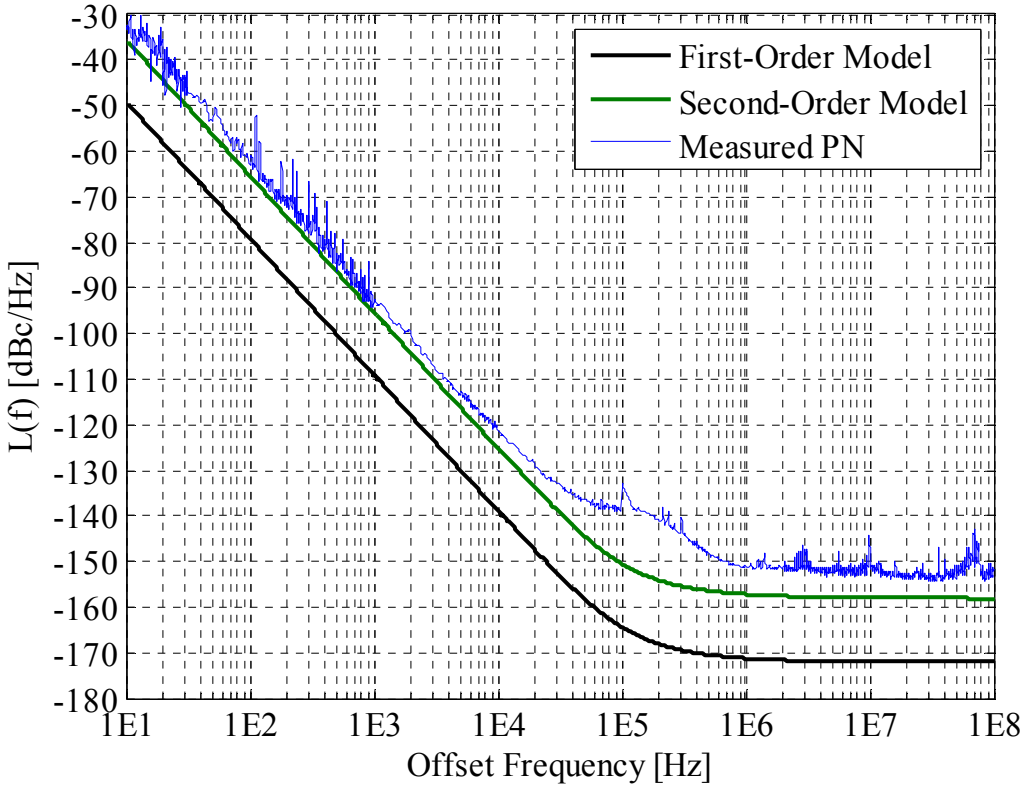


Fig. 6.15. 1st- and 2nd-order model fit to the phase-noise of the 1.006GHz oscillator

CHAPTER 7: Conclusion and Future Directions

This chapter discusses the contributions of this research study and briefly outlines the possible avenues that can be pursued for future research in micromechanical oscillators.

7.1 Contributions

This dissertation focused on the realization of high frequency micromechanical reference oscillators. As the result of this research effort, UHF tunable micromechanical reference oscillators were demonstrated; the major contributions to the technical field of micromechanical reference oscillator design are outlined here:

- A novel method to reduce the loss of capacitive micromechanical resonators without Q reduction is proposed. This is achieved by optimizing the thickness of the capacitive resonator for the minimum loss in the specific frequency. This research enabled a 145MHz capacitive SiBAR oscillator that meets the GSM phase-noise performance and to-date, is the highest frequency capacitive micromechanical oscillator reported in the literature.

- A detailed study of transimpedance amplifiers for series-resonant micromechanical oscillator applications was presented. This study covered basics of both open-loop and feedback TIA's in detail. Several gain and BW enhancement techniques with emphasis on their application in low-power high-frequency micromechanical oscillators were introduced. Finally some of these techniques were used to design and characterize several low-power high-gain CMOS TIAs capable of interfacing with micromechanical resonators with large shunt parasitic capacitance. Among these TIA's, one particular 0.18μm design took advantage of a low-power broadband

current pre-amplifier to boost the input current before converting that to voltage. This TIA showed the highest FoM among 0.18μm TIAs with similar BW. In addition, when interfaced with a high-Q 1GHz AlN-on-Si resonator, it demonstrated a low phase-noise 1GHz micromechanical oscillator with the highest reported FoM among the lateral micromechanical oscillators.

- Tuning methods for micromechanical oscillators were studied in detail. The study started with introduction of different frequency tuning methods: resonator-based and electronic and moved to determine the feasibility of electronic tuning for lateral micromechanical oscillators. Both parallel and series tuning techniques were investigated with emphasis on series tuning for series-resonant micromechanical oscillators. Limitations of series tuning techniques for series-resonant lateral micromechanical oscillators were identified; during this process, the role of shunt parasitic capacitance of the lateral micromechanical resonators in severely limiting the tuning range was highlighted. Shunt parasitic cancellation techniques were proposed and implemented with either active inductor or negative capacitor to improve the tuning range with minimal impact on the phase-noise performance of the oscillator. Finally, using the aforementioned methods, several 427MHz tunable oscillators were demonstrated with tuning range beyond 800ppm (when negative capacitance cancellation is used) and close-to-carrier phase-noise degradation less than 5dB across the entire tuning range. This research introduced the first-ever electronically-tuned lateral micromechanical oscillator.

- First-ever fully electronic temperature compensation of the high-frequency lateral micromechanical oscillator was made possible by the enhanced electronic frequency tuning mechanism developed in chapter 4. In this section, not only different temperature compensation methods such as material compensation are explained and supported by examples, the details of the circuits used for temperature compensation was also provided. These details included the bandgap and PTAT references, difference amplifier, linear V-to-I convertor, and square-root generator.

- Another contribution of this research study was the analytical phase-noise modeling of series-resonant lateral micromechanical oscillators. After introducing the basics of the phase-noise in oscillators and briefly introducing several well-known phase-noise models, this work focused on improving the LTI phase-noise model for high-frequency series-resonant micromechanical oscillators by considering the effect of parasitic capacitances. The effect of first-order and second-order parasitics of the amplifier and resonator were factored in to arrive at an improved LTI phase-noise model which was validated by measurement data for both capacitive and piezoelectric micromechanical oscillators.

7.2 Future Directions

A number of research areas can benefit from high frequency micromechanical reference oscillators. While the majority of these methods will take advantage of higher oscillation frequency to improve the overall system-level performance of radio transceivers, lately, there has been a strong willingness to pursue several interesting and rather unconventional research topics. These include taking advantage of nonlinear operation of

resonators for phase-noise improvement, single-resonator multi-frequency operation, ultra-stable micromechanical reference oscillators using a PLL-based closed-loop system, array of widely tunable micromechanical resonators for spectrum sensing. These topics are briefly discussed in this section.

7.2.1 Nonlinear Operation for Phase-Noise Improvement

According to the first-order LTI phase-noise model, the phase-noise of an oscillator whose resonating tank is a second order bandpass filter can be approximated as:

$$L(f_m) = \frac{kTF}{2P_{osc}}\left(1+\frac{1}{4Q^2}.\frac{f_{osc}^2}{f_m^2}\right)\left(1+\frac{f_c}{f_m}\right). \tag{7.1}$$

In practice, the sustaining amplifiers have finite input and output impedance and hence, load the resonator. If the resonator can be modeled as a series RLC tank and the sustaining amplifier is a transimpedance amplifier (TIA) with finite input and output resistance, the first-order approximation of the phase-noise is:

$$L(f_m) = \frac{kTF}{2P_{osc}}\left[1+\frac{1}{f_m^2}\left(\frac{f_{osc}}{2Q_L}\right)^2\right]\left(1+\frac{f_c}{f_m}\right), \tag{7.2}$$

where Q_L is the loaded Q of the resonator:

$$Q_{loaded} = Q_{unloaded}\frac{R_m}{R_m + R_{in} + R_{out}}, \tag{7.3}$$

where R_m, R_{in} and R_{out} are the motional resistance, input and output resistance of the amplifier, respectively. The noise of the parasitic cancellation blocks and tuning networks are included in F. It is clear from (7.2) that the close-to-career phase-noise can be improved by:

- Reducing the noise of the circuitry (including parasitic cancellation and tuning block)

- Reducing the flicker noise corner
- Increasing the loaded Q of the resonator
- Increasing the oscillation power

Since the phase-noise is normalized to the carrier power, increasing the oscillation power helps reduce the phase-noise. The oscillation power is both a function of the nonlinearity of the resonator and the amplifier. For linear operation, the oscillation power is limited well-below the power handling capability of the resonator; however, studies suggest that in nonlinear operation of the resonator, there exists a region in which the phase-noise of the oscillator can be lowered to a level just 3dB above the intrinsic noise of resonator when operating in linear region [89]. In this case, for sufficiently low-noise resonators (i.e. noise of the amplifier is at least 3× noise of the resonator and is the dominant noise source in the loop), the phase-noise of the oscillator with resonator operating in nonlinear region, can be approximated by double the noise of the same oscillator with noiseless amplifier and resonator operating in linear region. Using (7.2) developed for linear phase-noise approximation, the F can be approximated as 2 (3dB). This result is significant improvement for low-power CMOS oscillators as they are inherently noisy designs for gigahertz applications. The phase-noise improvement could be as much as 7-10dB in close-to-carrier.

As an example the 463MHz AlN-on-Si oscillator was driven into nonlinear region and its phase-noise is measured (Fig. 7.1). At $P_{osc}\approx$-5dBm, the close-to-carrier slope is higher than 30dB/dec, a strong indication for the presence noise sources other than the flicker

noise of the TIA in the output spectrum. The phase-noise is better than -92dBc/Hz at 1kHz offset which is around 3dB better than the when it is operating in linear condition. Future studies may reveal potential for more much-needed phase-noise improvement.

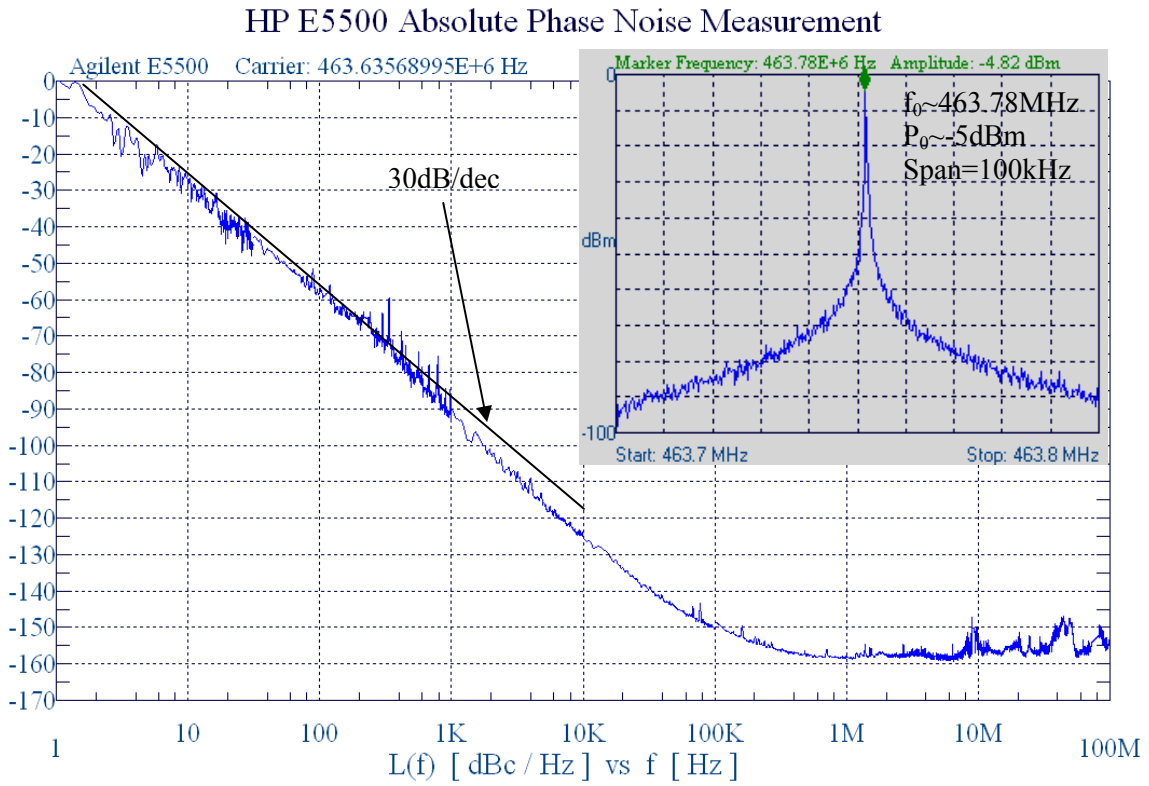


Fig. 7.1. Spectrum and phase-noise of the 463MHz oscillator in nonlinear region

7.2.2 Single-Resonator Dual-Frequency Micromechanical Reference Oscillator

Multi-mode radio transceivers are becoming increasingly popular as standard platform for simultaneous voice, data, and multi-media communications in a single chip [3], [4]. Due to the inherent in-compatibility of the fabrication process of quartz crystal resonators with silicon, designers are forced to compromise on system performance by relying on a single reference oscillator to generate multiple frequencies. Lateral micromechanical resonators such as SiBAR and TPOS enable the integration of multiple resonators with

different fundamental frequencies on the same substrate; thus allowing for optimization of the transceiver performance in each band.

Dual-frequency oscillators have shown excellent performance in accurate sensors and highly-stable reference oscillators for multi-mode wireless transceivers [90], [91]. The difference in the phase-noise requirement of narrowband 2G standards such as GSM [8] and OFDM-based 3G/4G [3], [4] standards calls for multiple reference oscillators, each optimized for a specific standard [1]. Using a dual-mode resonator helps achieve this goal while maintaining the same form factor and potentially lowering the cost.

High-order TPOS resonators exhibit a unique behavior in which both the fundamental and higher-order response can be exploited to create dual-mode oscillators [65]. A cascade of inverting and/or non-inverting stages can produce the required 0º or 180º needed for oscillation in different modes. An on-chip switching network can be used to change the oscillation frequency accordingly. Exploiting 180º phase difference between fundamental and higher order mode, no precautions need to be taken for mode-suppression in the loop (Fig. 7.2).

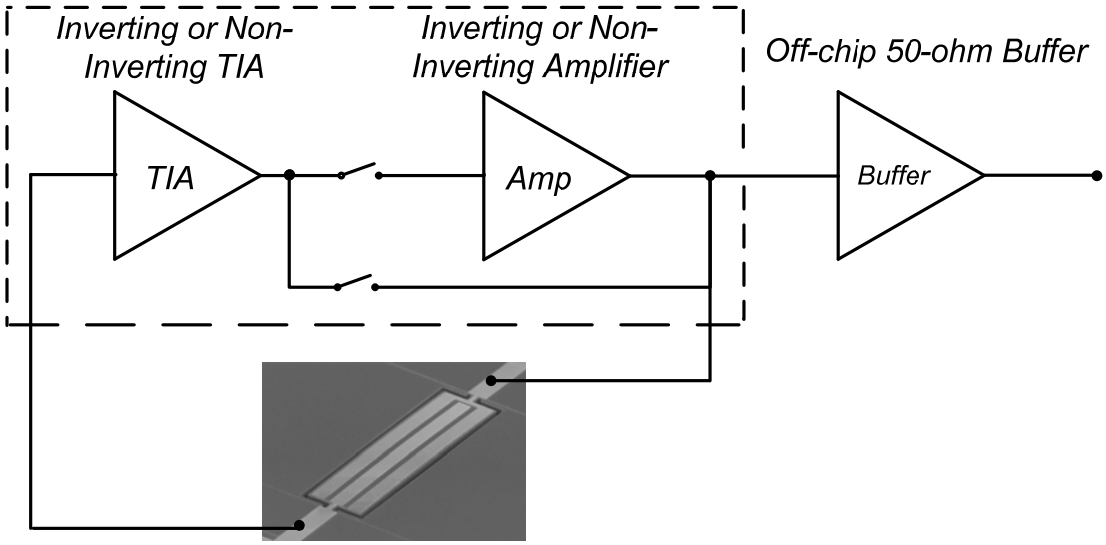


Fig. 7.2. Block diagram of the single-resonator dual-frequency TPOS oscillator

Using a $1^{st}/5^{th}$ mode TPOS resonator operating at 35MHz and 175MHz (Fig. 7.3) with the RGC TIA of chapter 3 combined with a switching network (Fig. 7.4) for mode selection, a dual-mode micromechanical oscillator can be created.

The oscillation spectrum and phase-noise in both modes have been monitored for both oscillation modes (Fig. 7.5 and 7.6).

The phase-noise results are comparable with miniaturized crystal oscillators raising the hope for increased functionality and performance in future advanced multi-mode radio transceivers.

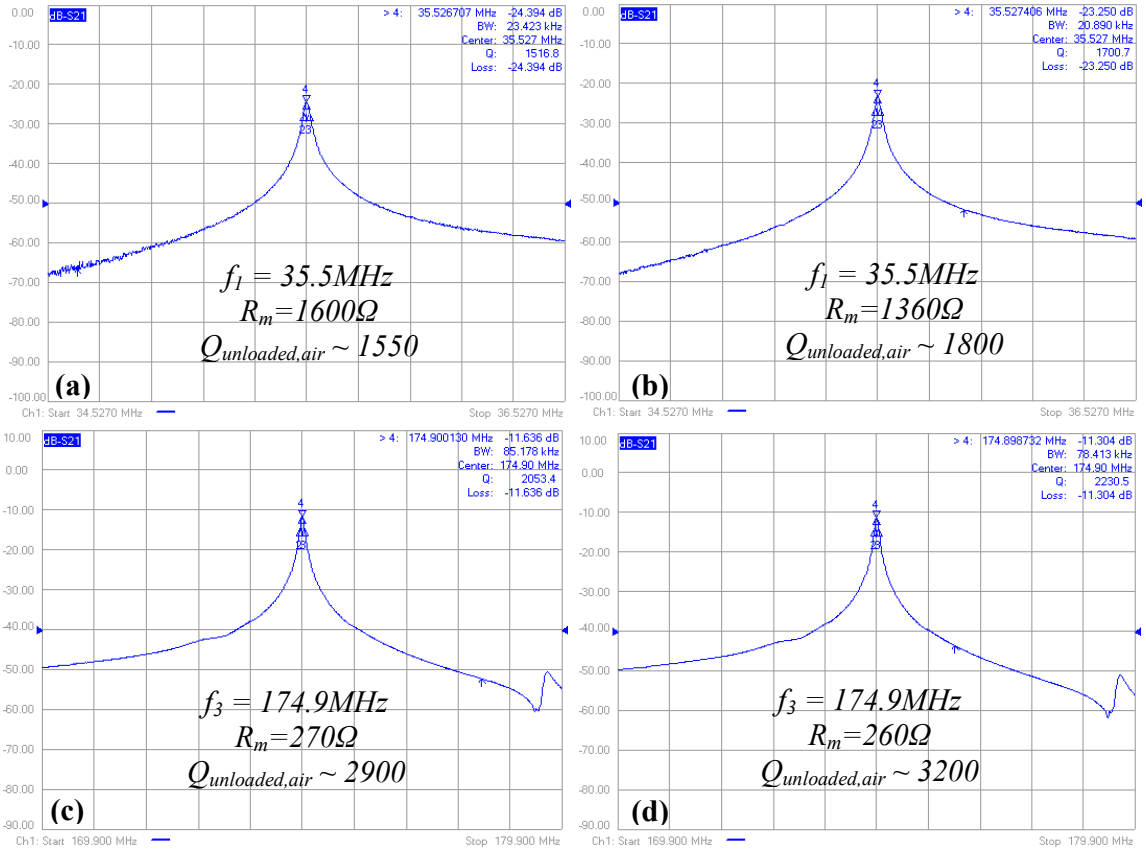


Fig. 7.3. Response of the 1st/5th order resonator: air, (a), (c) and vacuum, (b), (d).

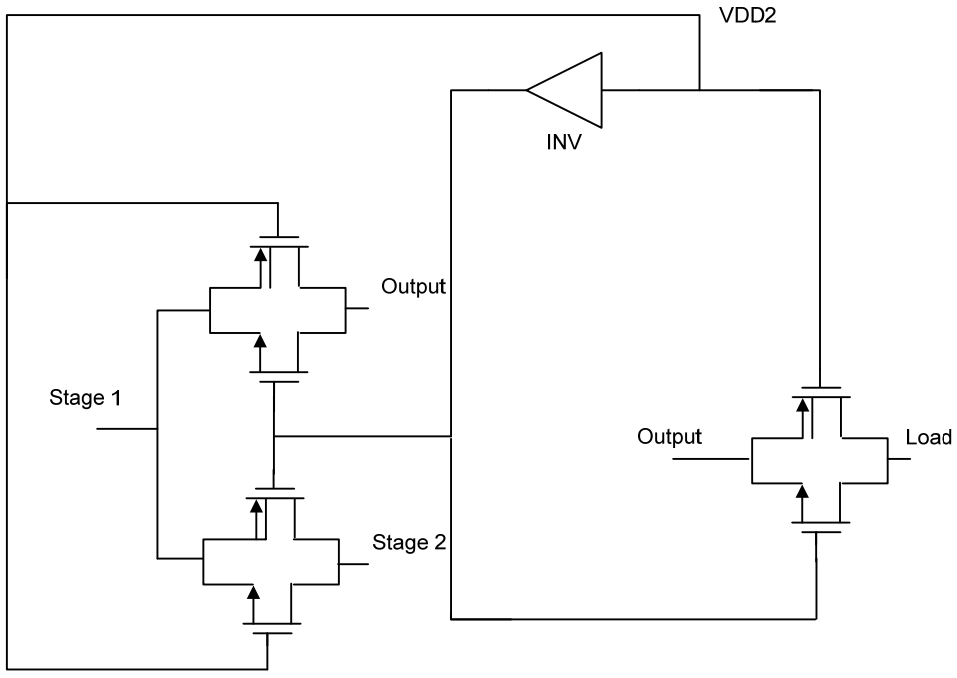


Fig. 7.4. The block diagram of the switching network

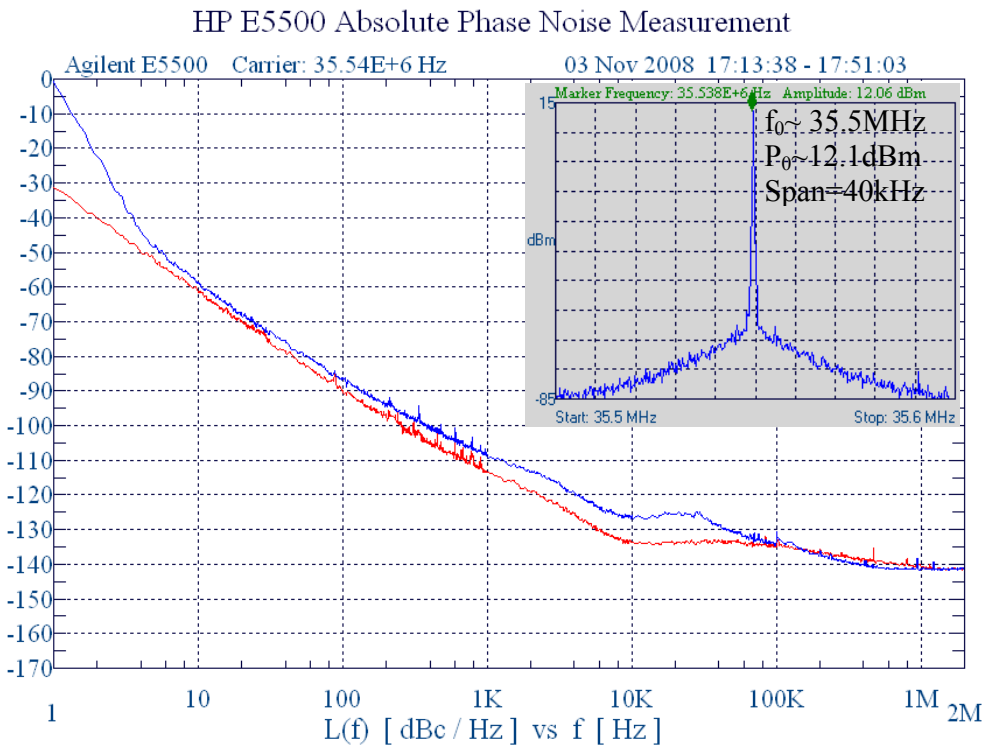


Fig. 7.5. Phase-noise and spectrum of fundamental mode of the 1st/5th oscillator

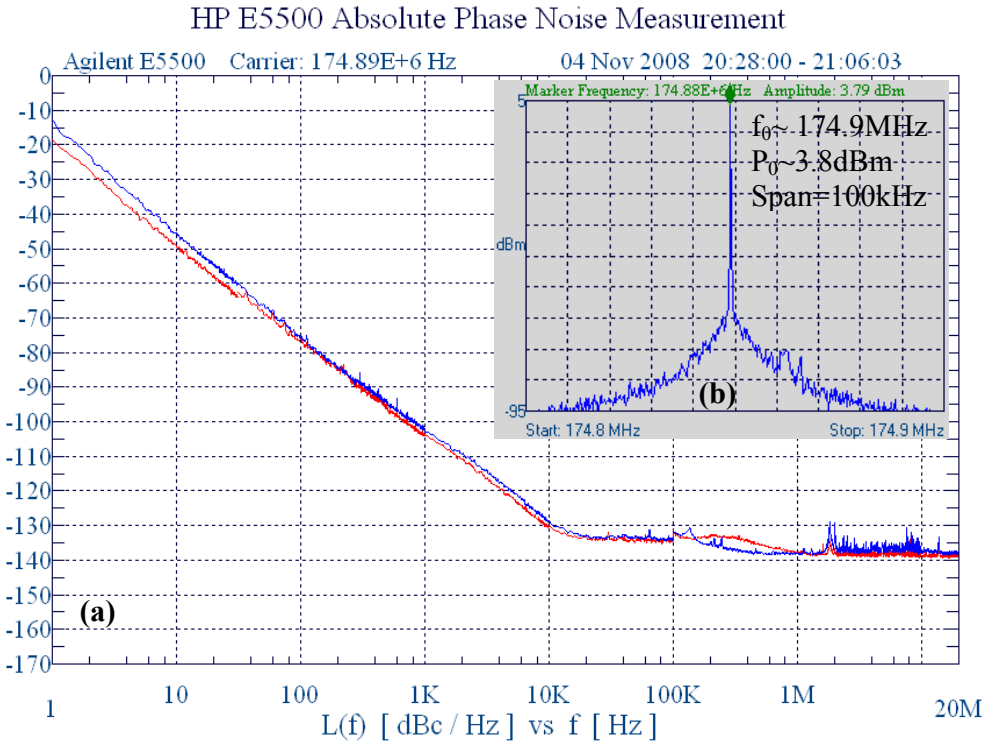


Fig. 7.6. Phase-noise and spectrum of higher order mode of the 1st/5th oscillator

7.2.3 Ultra-Temperature-Stable PLL-Based MEMS Reference Oscillator

Recent radio transceiver applications require ultra temperature-stable reference oscillators with stability requirement comparable to ±1ppm oven-controlled crystal oscillators (OCXO) [92]. Since the main source of error in open-loop temperature compensation circuits are the absolute error of building blocks which cannot improved beyond a fundamental limit due to process variation, it is wise to pursue a closed-loop temperature compensation to deliver ultra temperature-stable (±1ppm) reference oscillators. Most closed-loop architectures use PLL-based architecture in which the frequency of the output signal is tracking a fixed reference frequency with a small pre-determined error.

In the PLL-based temperature compensation architecture, the temperature compensation is achieved by: first accurately measuring the frequency drift of the oscillator within -40ºC to 85ºC range and storing this information in a look-up table; then, using the pres-stored information in a high resolution fractional-N frequency synthesizer to reduce the overall drift to ±1ppm. Obviously, there are risks associated with the accuracy of the PLL loop itself. Dynamic temperature compensation is one of the promising methods that can be used to mitigate this risk.

The oscillation frequency of the micromechanical oscillator is seldom equal to its intended designed value. To allow on-the-fly pulling mechanisms, frequency-synthesizers offer a simple but effective way to bring the frequency to its intended value. In addition, PLL-based frequency synthesizers provide noise filtering. When the offset frequency is small, fractional-N PLLs become the preferred option to trim the frequency.

Several options have been proposed to construct the fractional divider; however, it has been demonstrated that the system based on a higher-order ΣΔ-modulator is able to minimize the incidence of constant inputs, which is usually the case for fractional dividers. The constant input will be called calibration factor (K). When perturbation sources are added to the reference source and the offset frequency cannot be determined a priori, the option of tuning operating frequency on-demand is more attractive. For fractional-based PLL, the on-demand trimming can be done by modifying the calibration factor (K), which changes the fractional division ratio.

When the variation of the operating frequency with respect to temperature is considered, the calibration factor cannot be fixed and must be changed accordingly. Since the frequency change vs. temperature can be fully characterized and it is relatively constant, the PLL-based frequency synthesizer will be extended to include a sensor that associates the current temperature to a value of the calibration factor thru a look-up table. The calibration factor will be 20-bits long which allow mapping the frequency range into 1,048,576 different calibration factors. Fig. 7.7 shows a general block diagram of the dynamic closed-loop temperature compensation system.

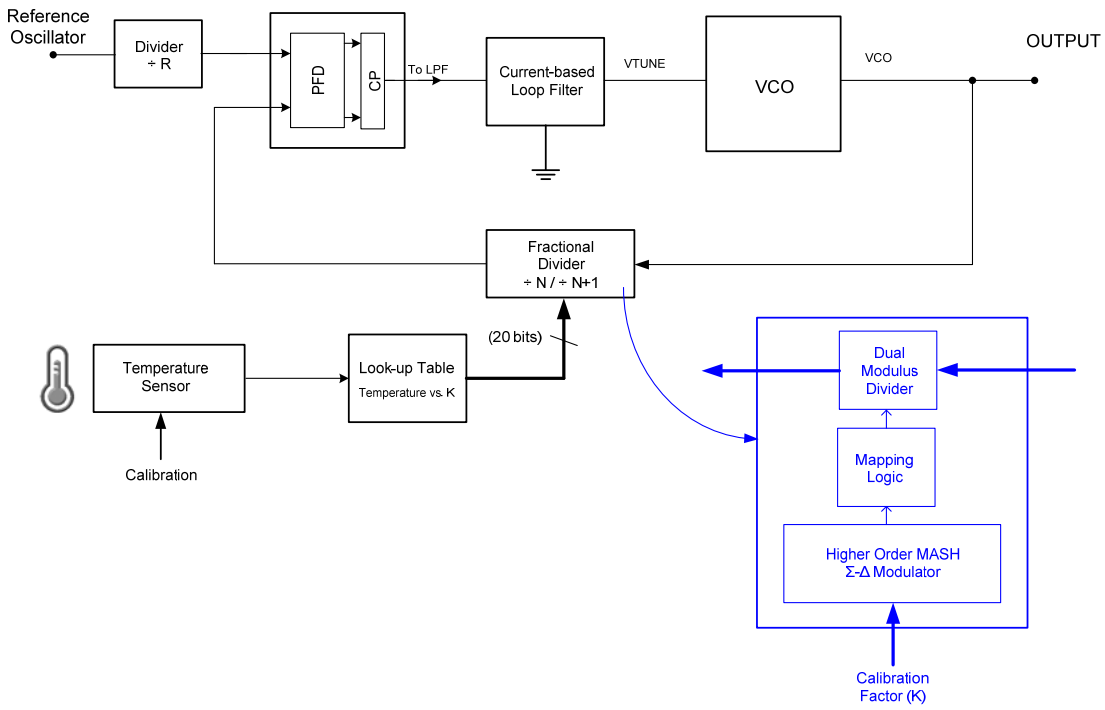


Fig. 7.7. Diagram of the dynamic closed-loop temperature compensation

7.2.4 Resonator-Based Mechanical Spectrum Analyzer

Building a compact spectrum analyzer with wide range and fast sweep capability has amazed microwave engineers since the early days of RF electronics. Almost all commercially-available spectrum analyzers are built based on swept-tuned architectures in which one or more filters are tuned to scan the entire frequency spectrum (Fig. 7.8). While swept-based spectrum analyzers are easy to implement, they suffer from long sweep time and inherent limitation in the accuracy of the measurement that is determined by the IF filter bandwidth. High-Q lateral micromechanical filters, on the other hand, provide high resolution with capability to realize multiple equally-spaced frequencies on the same substrate in a compact area. Fig. 7.9 shows a proposed mechanical spectrum analyzer that uses an array of individually-tuned lateral mechanical filters in zero-IF configuration. This architecture allows for simultaneous spectral processing at all

frequencies, effectively making it a parallel spectrum analyzer with near-zero sweep time. Additional tuning on each filter can reduce the number of filters to less than 100 for the UHF band.

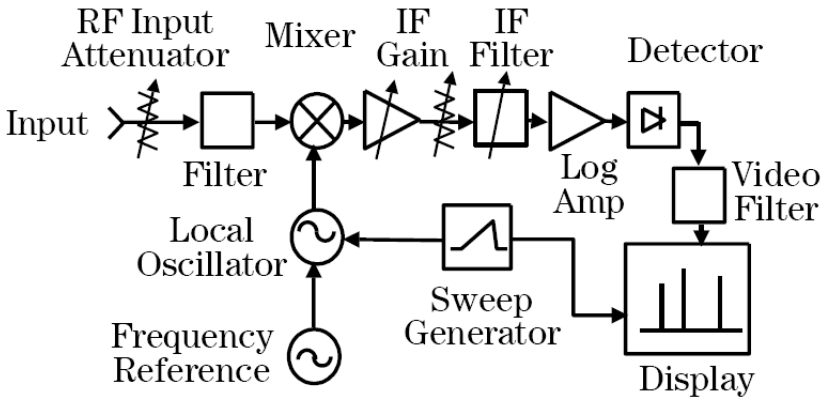


Fig. 7.8. General block diagram of the swept-tuned spectrum analyzer

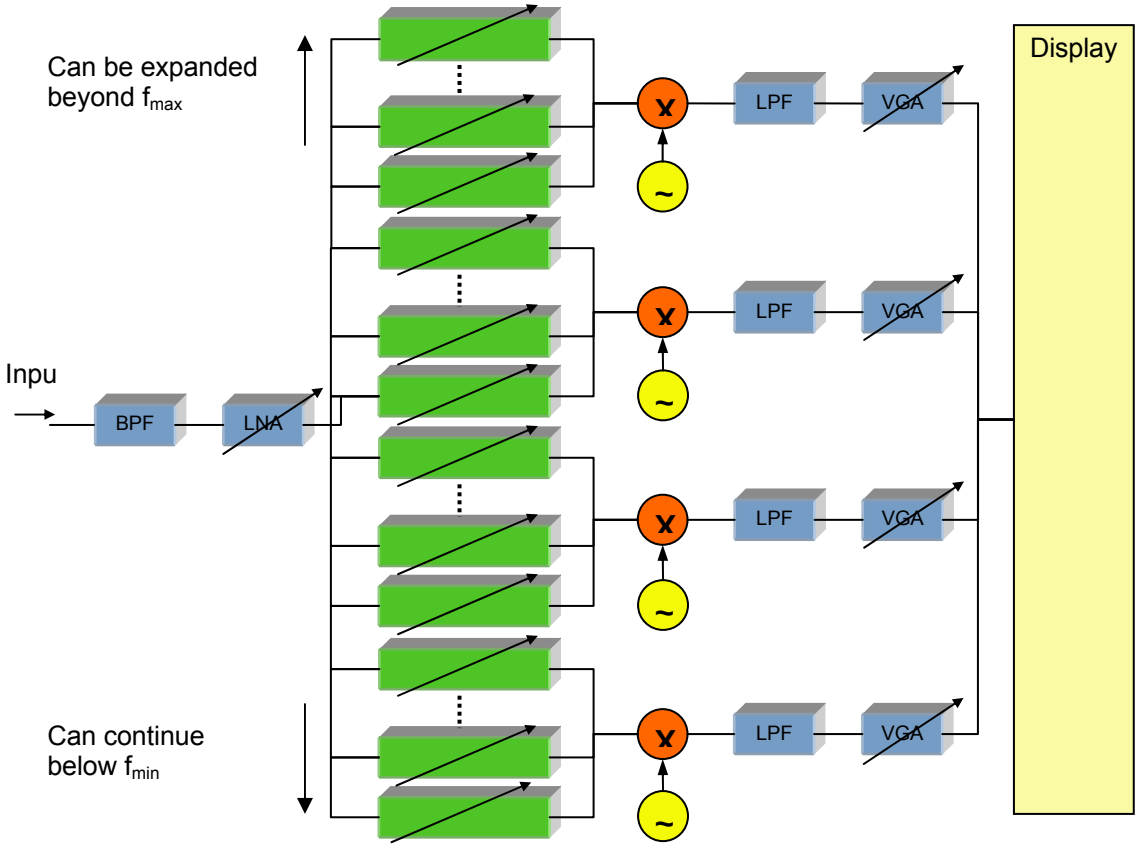


Fig. 7.9. General block diagram of the mechanical spectrum analyzer

7.3 Conclusion

This chapter summarized the main contributions of this research work to the body of the technical knowledge in the field of micromechanical reference oscillator design and characterization. In addition, it provided valuable insight into the future directions that can be pursued to improve the performance and functionality of modern transceivers as well as spectrum sensing.

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